High-Speed Electronic Circuits
for 100 Gb/s Transport Networks

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Abstract: An overview of state-of-the-art high-speed electronic circuits for major 100G modulation schemes is given. The results show the trade-off between electrical performance and energy efficiency and lead to design considerations for future transceiver electronics.
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1. Introduction

100G Ethernet technology is still under development but has entered a stage where electronic components are selected according to their competitive potential at product level. That is, besides the electrical performance also low power consumption (energy efficiency), integration and reconfiguration capability, reliability and cost become important design criteria. As high-speed operation is in general supported by high operating currents, power saving is a big challenge in the development of high-speed circuits for the transceivers with their various coding schemes under discussion (e.g. OOK, DP-QPSK, OFDM). This holds especially for those circuits where performance close to the feasibility limit is required. Apart from circuit concepts this limit depends strongly on the choice of semiconductor technology, the partitioning, and the related component interfaces. Furthermore, specifications can be relaxed by either shifting performance requirements from one chip to another with a higher capability or by compensating for deterministic performance degradations by algorithms within the DSP. All these criteria together with the possible degrees of freedom make transceiver development a rather complex task where fix points and boundary conditions are helpful for orientation. This work shall support orientation by presenting an overview of state-of-the-art high-speed electronic circuits together with performance, power consumption, and technology considerations (Sect. 2, 3, and 4). Sect. 5 draws some conclusions and proposes a possible development strategy.

2. SerDes components, Multiplexer (Mux), Clock and Data recovery with Demultiplexer (CDR&Demux)

For the Mux circuits in Tab. 1 those with bipolar transistors and direct selector output have the highest inherent speed potential of all lumped circuit concepts discussed in this work (cf. [14]). In III-V InP technology record rates of 165 Gb/s are achieved [46] that can be traded for lower power consumption and higher voltage swing (cf. Tab 1).

Table1. Some state-of-the-art MUX and CDR&Demux results.

	MUX					CDR&Demux				
	BR/ Gb/s	V_{out} /mV$_{pp}$	P/ W	type, f_t/f_{max} /GHz	Ref.	BR/ Gb/s	V_{min}/ V	P/ mW	type, f_t/f_{max} /GHz	Ref.
III-V HBT (InP)	165	400	1.6	4:1, >300/300	[46]	100	120	2100	1:2, > 300/300	[8]
	100	700	0.8	speed/power trade-off						
SiGe HBT, BiCMOS	132	500	1.45	4:1, 210/n.a.	[47]	107	80	5000	1:2, 180/200	[10]
	86	600	0.85	8:1, 150/150	[3]					
CMOS	60	100	0.01	2:1 selector, 90nm	[4]	81	80	200	TIA & full-rate latch, 65nm	[11]
	50	200	0.1	2:1, 130nm	[5]	40	n.a.	57	1:1 CDR (retimer), 90nm	[12]
	40	400	0.13	4:1ext. clk, 90nm	[6]	40	n.a.	48	1:2, 90nm	[30]
	40	560	0.33	4:1& intl.CMU, 90nm	[7]	40	n.a.	2800	1:16 SFI-5, 65nm	[13]
	40	800	2.8	16:1 SFI-5, 65nm	[13]					

Bitrate (BR), differential outp. volt. (V_{out}), power (P), transistor transit / maximum oscillation frequency (f_t/f_{max}), min. input voltage (V_{min}).

The same can be done in SiGe designs that are able to operate up to 132 Gb/s in state-of-the-art BiCMOS technology [47]. However, a certain speed overhead should be preserved to comply with production requirements for yield and reliability. Sufficient high speed to trade with power is expected to come from next generation 500 GHz SiGe bipolar transistors, currently under investigation (cf. e.g. www.dotfive.eu). Probably as a consequence of high data/clock rate and high voltage swings required in the final Mux stage, CMOS designs are struggling with data rates above 40 Gb/s. Only a rudimentary selector core reaches 60 Gb/s [4] aiming at demonstrating a low power consumption, which, however, rapidly increases by circuit complexity [4-7,13]. Finally,

a pure CMOS SFI-5 compliant MUX [13] consumes more power than commercially available 40G standard products in 130 nm SiGe-BiCMOS technology (cf. e.g. SMI4027, Sierra Monolithics).

The same conclusion holds for the CDR&Demux circuits in Tab. 1, which consume at 100 Gb/s more power than the Mux because a greater portion of circuitry is running at a speed close to the feasibility limit [8,10]. Remarkable results are obtained for CMOS retiming circuits [11,12,30], which massively exhaust the gain peaking capabilities of large on-chip inductors/transformers in combination with low supply voltages.

From the results it is expected that future SerDes designs can become more energy efficient if state-of-the-art BiCMOS technologies are applied and, besides the CMOS part, also the bipolar part adopts applicable energy saving techniques. If next generation BiCMOS technologies offer a sufficient speed potential to trade for low power consumption, a 100G SerDes chipset with 4x28 Gb/s interfaces could target 2W total power consumption.

3. Amplifiers

Tab. 1 shows that modulator drivers realized as distributed amplifiers in InP DHBT (also true for HEMTs) technology offer single-ended output voltage swings in excess of $2V_{pp}$, and sufficient bandwidth and gain for 100 Gb/s operation at reasonable power consumption [15]. Generally this distributed type of amplifier has linearized

Table 2. Some state-of-the-art amplifier results.

	Driver					TIA					AGC				
	BR/BW Gb/s/GHz	V_{max}/G/type /V_{pp}/dB/ -	P / W	f_t/f_{max} / GHZ	Ref.	BR/BW / Gb/s/GHz	Z_{TI} / dBΩ	P / mW	f_t/f_{max} / GHZ	Ref.	BW/ GHz	G_{max}/G_{min} /dB	P / mW	f_t/f_{max} / GHZ	Ref.
III-V HBT (InP)	100/120	2.3/21 /ds	0.61	350/370	[15]	40/60	71	271	150/200	[23]	36	22/3	814	150/120	[32]
	n.a./110	2.8/17 /ds	0.22	337/345	[16]	43/35	75	450	160/160	[24]					
	40/50	11.3/25 /dd	3.0	150/200	[17]	40/49	48	286	170/140.	[25]					
SiGe HBT	40/32	2.5/13 /dd	0.23	80/90	[18]	84/80	54	1W	180/250	[26]	48	21.5/0	1200[3]	122/163	[33]
	40/22	7.2[1]/42 /dd	3.6	160/160	[19]	56/35	72	211	200/250	[27]	30	11/0	560	75/95	[45]
	50/n.a.	2.0/Pmux	2.0	72/75	[14]	40/50	49	182	200/n.a.	[25]					
CMOS	n.a./80	n.a./7.4 /ds	0.12	90nm	[20]	n.a./70	44	200	130nm	[28]	22	26/7	75	90nm	[30]
	40/33.4	1.6/16 /ds	0.26	180nm	[21]	40/31	51	60	180nm	[29]					
	40/39.4	1.3/20 /ds	0.25	"	"	40/22	66	75[2]	90nm	[30]					
	n.a./90	2.5/11 /ds	0.21	120nm SOI	[22]	25/20	70	70	65nm	[31]					

Bitrate (BR), bandwidth (BW), driver type distributed differential/single ended (dd/ds), max. differential (dd) /single ended (ds) output voltage swing (V_{max}), gain (G), transimpedance (Z_{TI}), for 50-Ω input: Z_{TI} =voltage gain + 34 dB, max./min. voltage gain (G_{max}/G_{min}), [1] 75Ω driver, [2] TIA and AGC, [3] additional 1.6 W are consumed by a full-wave rectifier.

gain stages suitable for multilevel or even analog modulation schemes. At the lower bandwidths of such schemes significantly higher output voltages can be obtained [17], though not necessary if future 100 Gb/s modulators operate with driving voltages well below $2V_{pp}$ [1,2]. This enables also the application of (almost) linear, distributed SiGe and CMOS drivers [18-22] that offer >$2V_{pp}$ voltage swing up to 40 Gb/s/30 GHz in differential (push-pull) configurations. Energy efficiency and signal performance can be improved if driving voltages below $1V_{pp}$ are allowed. In this case the analog DAC output voltage ($1.6V_{pp}$, Tab.3 [35]) is sufficiently high to drive directly the modulator. Digital voltage swing at 100 Gb/s can be increased by utilizing the power-Mux concept [14].

Real transimpedance amplifiers (TIA) [23-25,27] in Tab. 2 use parallel feedback technique to achieve a low input impedance («50Ω) that improves bandwidth and input sensitivity. As feedback quality is reduced at higher speed and matching of 50-Ω photodiodes is required, amplifier without feedback can be applied [26,28-30]. From Tab. 2 and from a comparison in [25] SiGe bipolar technology offers superior performance for the TIA. Cost and size of the receiver can be improved by a higher integration level, e.g. 4x25Gb/s TIA [31]. Interface power can be saved if there is an AGC amplifier that can be integrated together with the TIA [30] (or with the ADC).

Amplifiers with automatic gain control (AGC) experience a renaissance as they help to exhaust the full vertical resolution of the succeeding ADC by keeping the ADC input amplitude at full scale, i.e. independent of the varying intensity of the received signal. Best results achieved in comparatively slow SiGe technology [33, 45] demonstrate the feasibility to create such amplifiers with sufficient bandwidth and point out a large power saving potential if much faster state-of-the-art technologies were applied. Imperfections in the frequency dependent transfer function can be compensated for by algorithmic post-processing in the DSP if their dependency on the gain setting is known.

4. Conversion between analogue and digital domain

Recent developments [34,35] of very fast digital-to-analog converters (DAC), shown in Tab. 3, achieve sampling rates in excess of 30 GS/s and a physical resolution of 6 Bit. As a figure-of-merit to characterize

Table3. Some state-of-the-art converter results.

	DAC				ADC			
	SR/Res GS/s / -	t_r/V_{fs} ps/V	P / W	f/f_{max}, Ref / GHz / -	SR/f_{ENOB} / GS/s/GHz	Res / ENOB	P / W	f/f_{max}, Ref / GHz/ -
III-V HBT	32/6	30/0.3	1.4	175/260, [34]	24/10	3/2.3	3.8[2)]	150/240, [39]
SiGe HBT, BiCMOS	34/6	<12/1.6	12.5	200/250, [35]	35/8	4/3.2	4.5	160/n.a., [40]
	20/8	>24[1)]/0.8	2.5	190/190, [36]	30/22	6/4.0	10	200/250, [41]
	20/6	n.a./1.0	0.36	150/200, [37]	20/10	5/3.5	4.9	200/250, [42]
CMOS	12/8	>31[1)]/1.0	0.19	90nm, [38]	56/17	8/5.68	4	65nm,[43]
					24/12	6/4	1.2[2)]	90nm, [44]

Sampling rate (SR), physical resolution (Res), 20%-80% rise/fall-time (t_r) at full-scale swing (V_{fs}), effective number of bits (ENOB) at f =(f_{ENOB}), [1)] 0.22/resolution bandwidth, [2)] with decoder logic.
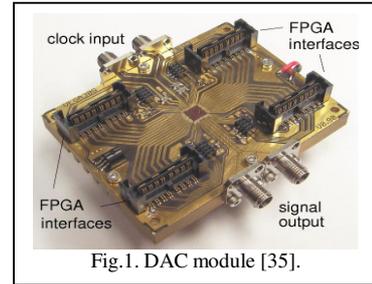

Fig.1. DAC module [35].

the high-speed performance of a DAC in time domain, its ability to perform a full-scale voltage step within one sample period can be used. Tab. 1 provides rise/fall time and the related full-scale voltage swing, partly based on calculations or estimations in the absence of explicit numbers. Excellent results [35] are obtained in SiGe technology but at a high power consumption of which 30% are caused by the high-speed DAC core and 70% by the 24x7Gb/s interface for FPGA synchronization, cf. Fig. 1. While a realization of the DAC in CMOS technology does not show sufficient speed so far, record sampling rate and resolution is announced for a CMOS ADC [43] but without power consuming real-time interface to an FPGA. In contrast, the SiGe DAC [41] was designed for high bandwidth and real time FPGA operation to enable early system experiments at cost of a high power consumption.

Next steps towards energy efficient real-time converter solutions may follow two different approaches. The mainstream approach is the complete realization of converter and DSP in CMOS technology. If both circuits are integrated on the same chip the trade-off between DSP and ADC requirements may jeopardize overall performance. Anyway, the result is a large digital IC with a high-speed analog input. Alternatively, the best of two worlds in terms of energy efficient digital logic and high-speed analog performance can be combined if the high-speed converter front-end is realized in SiGe-bipolar technology and CMOS is used for the high gate-count digital circuitry of the converters and the DSP. This strategy is considered for power reduction in the next development steps of the SiGe converters [35, 41]. Besides a realization of the plain converters in state-of-the-art BiCMOS technology also integration of converter and DSP can be achieved by a 2D or 3D system in a package assembly, potentially together with the electro-optical converters. For chip-to-chip signaling over the very short distances in the package, energy efficient parallel 25/28 Gb/s interfaces can be applied [48]. However, adequate measures for thermal management of such an assembly have to be considered. For power saving integration of ADC and probably also the DSP, next generation BiCMOS technology appears to be a viable option as it could offer both, 500 GHz bipolar transistor speed and 65 nm CMOS on the same chip.

5. Conclusion and outlook

State-of-the-art high-speed circuits show enough performance for operation in 100G Ethernet transceivers. However, power consumption is far too high and best results are obtained in different technologies. Following the trend in low driving-voltage modulators, the whole high-speed transceiver electronics can be realized in state-of-the-art SiGe-bipolar and CMOS technology. Depending on integration, cost and flexibility aspects both technologies can be combined either by a 2D or 3D chip assembly or by applying state-of-the-art BiCMOS technologies. A significant step towards higher integrated, energy efficient, low cost transceivers can be enabled by future BiCMOS technologies if bipolar transistor speed is high enough to trade for low power consumption and the CMOS part is suitable for integration of fast high gate-count logic, potentially including the DSP.

6. Acknowledgement

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