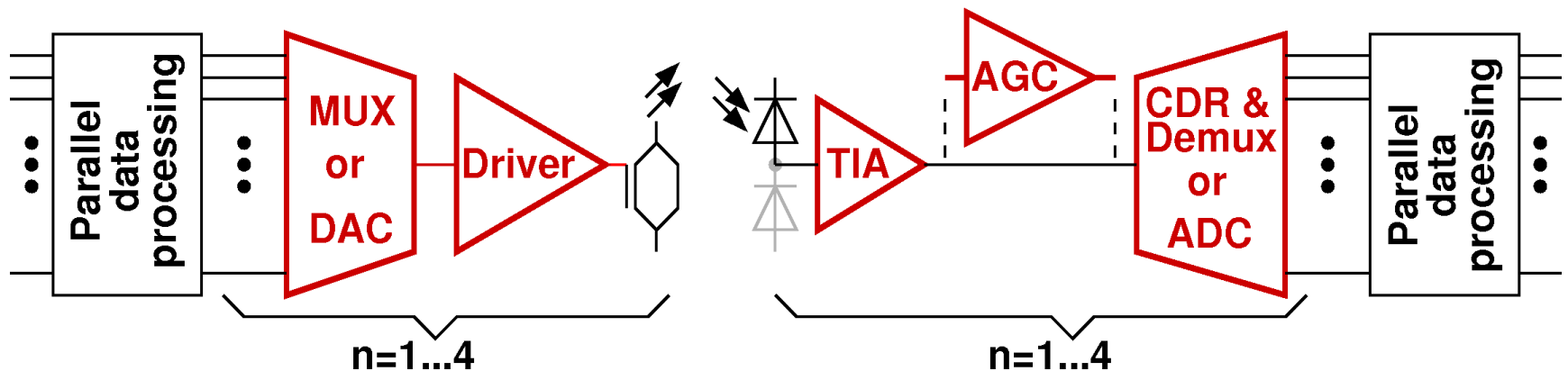
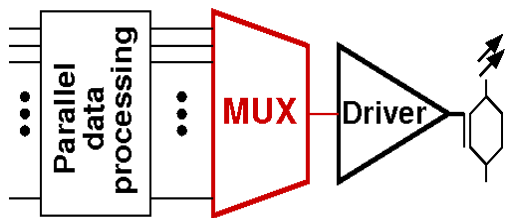

High-Speed Electronic Circuits for 100 Gb/s Transport Networks

Michael Möller & team members & partners
Dep. of Electronics and Circuits,
Saarland University, Germany, and
MICRAM Microelectronic GmbH, Germany

Motivation & Outline

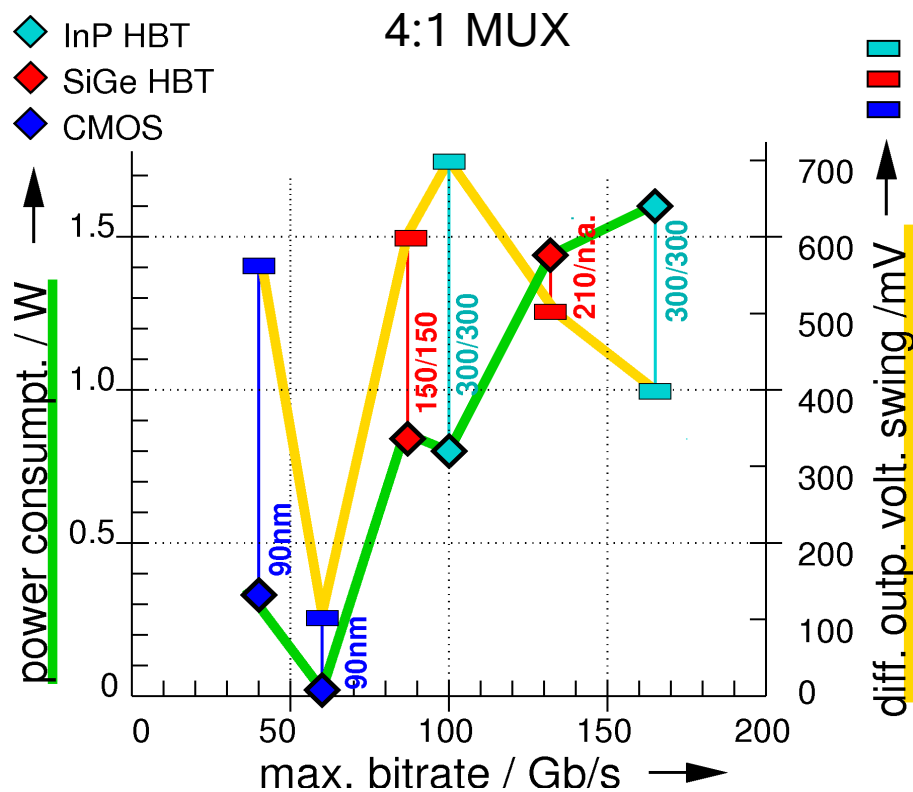
- Develop the “best” high-speed 100G electronics solutions
- Consider SiGe: Inherently fast, high performing, cheap, homogeneous integration (Bi+CMOS), energy efficient
- Outline:
 - State-of-the-art & design considerations
 - Actual SiGe ADC and DAC demonstrators
 - Outlook



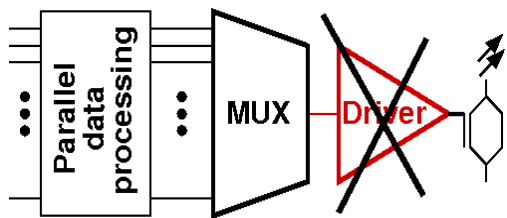


Digital (OOK) MUX

- Fastest device on earth
 - InP HBT MUX
165 Gb/s, 400 mV_{pp}, 1.6 W
 - High speed allows trade-off:
100 Gb/s, 700 mV_{pp}, 0.8 W
- SiGe speed is sufficient:
132 Gb/s, 500 mV_{pp}, 1.45 W
- MUX output selector is inherently fast(est circuit)
- Speed supported by $g_m \uparrow$
~ gain & output conductance
- CMOS ($g_m \downarrow$) < 50 Gb/s

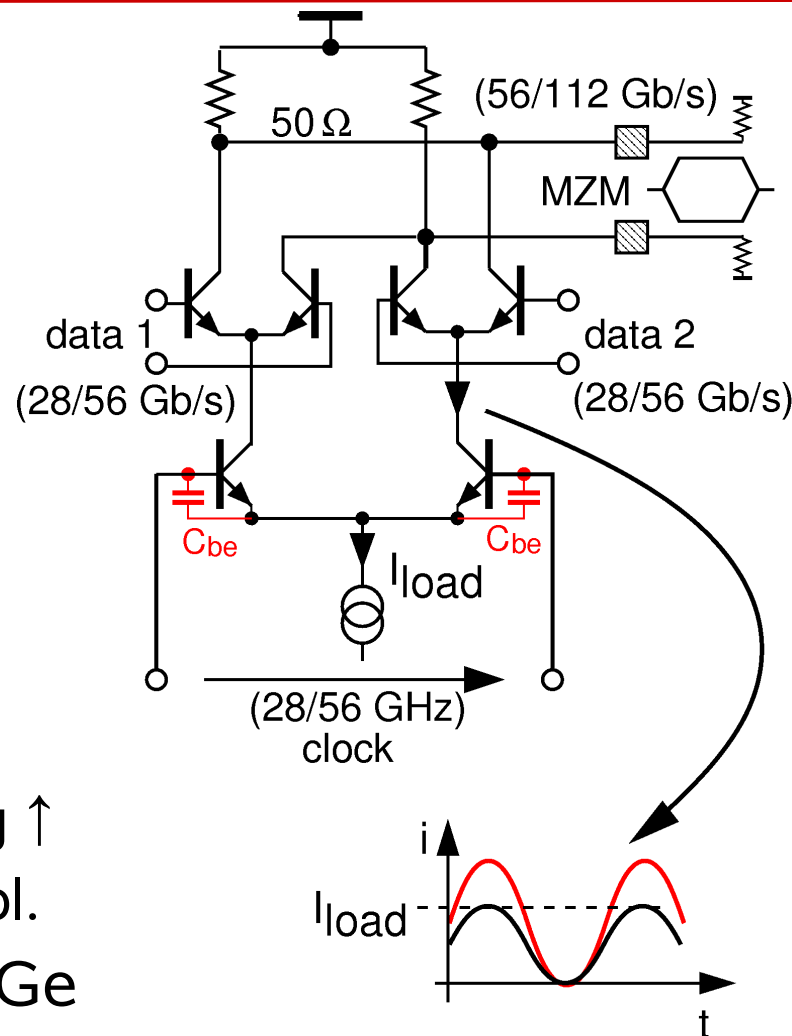


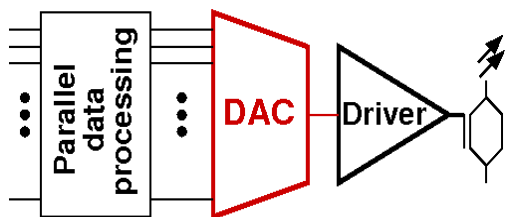
$$\text{HBT } g_m(I_0) \approx 10 \text{ MOS } g_m(\sqrt{I_0})$$



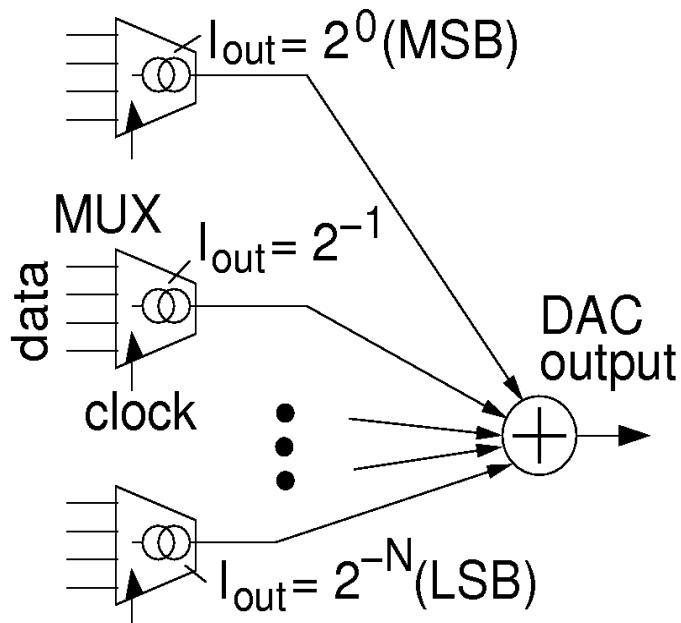
Digital Modulator Driver

- Aim: power + cost saving
- Consider: MZI, $V_{\pi} = 2$ V, push-pull config.
- Direct drive by Power-MUX:
 - ✓ 50 Gb/s, 2 V_{pp} (1998)
(Si-bipolar $f_t/f_{\max} = 72/75$ GHz)
- Standard MUX
 - 0.7 V_{pp} @ 100 Gb/s (InP)
 - 0.5 V_{pp} @ 132 Gb/s (SiGe)
 - to be optimized for voltage swing ↑
 - support by next gen. HBT technol.
- Expect > 1 V_{pp} @ 112 Gb/s in SiGe

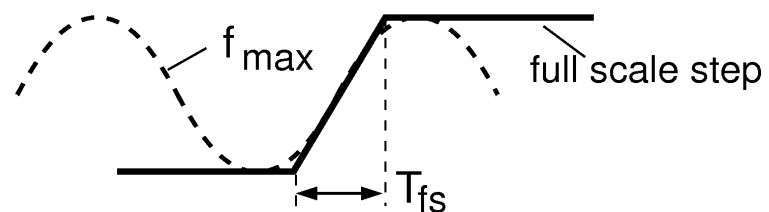
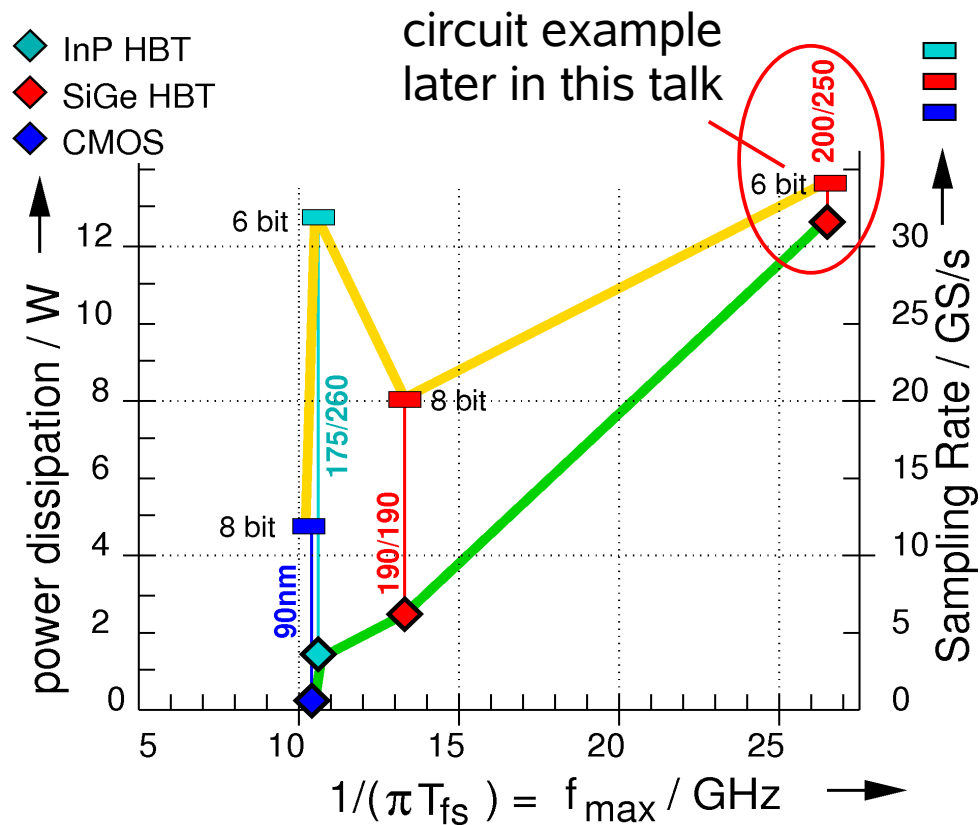


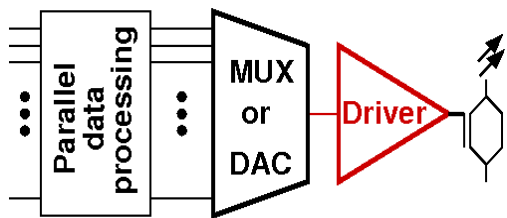


Analog MUX: DAC



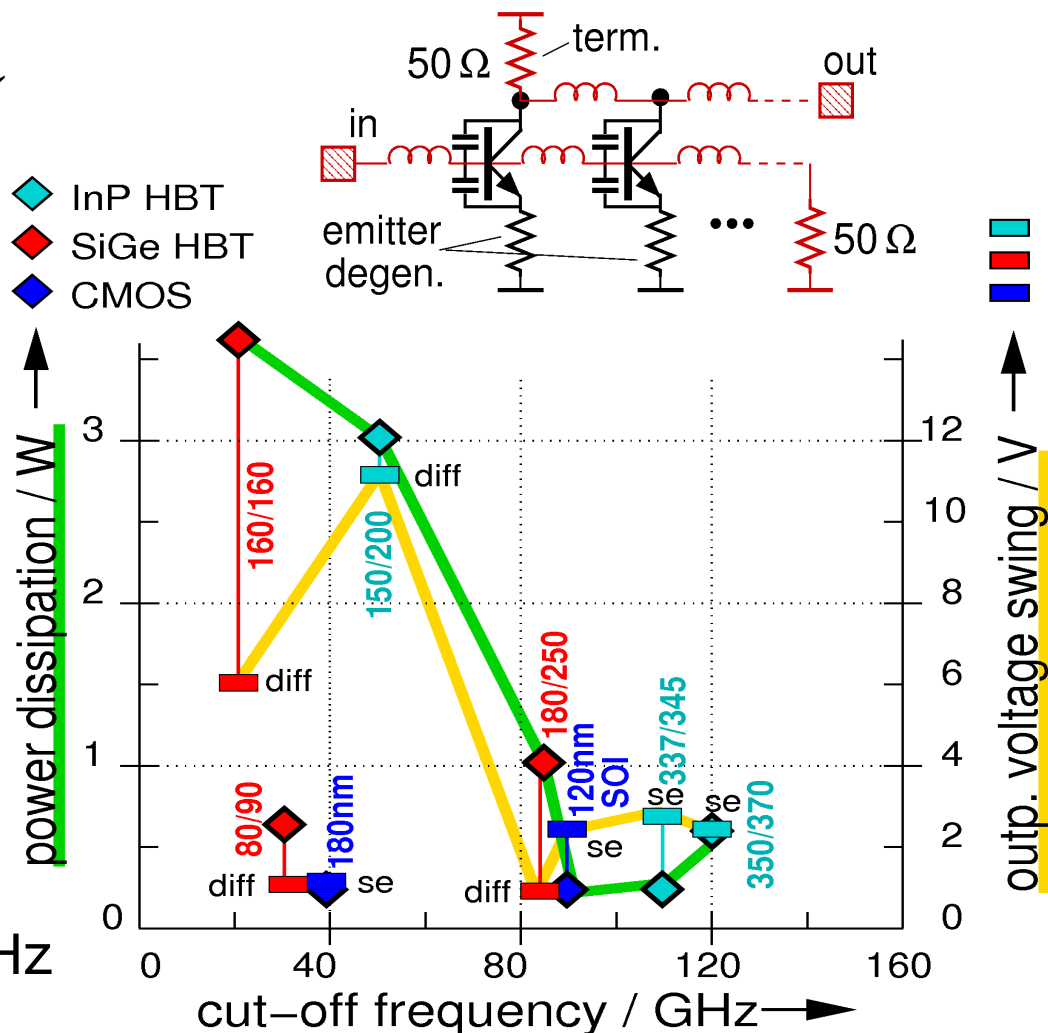
- MUX concept enables very fast SiGe DACs
- Direct push-pull modulator drive with $2 V_{pp}$ @ 30 GHz possible

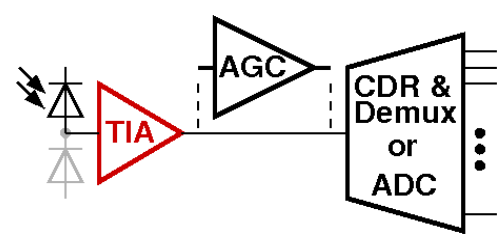




Linear Modulator Driver

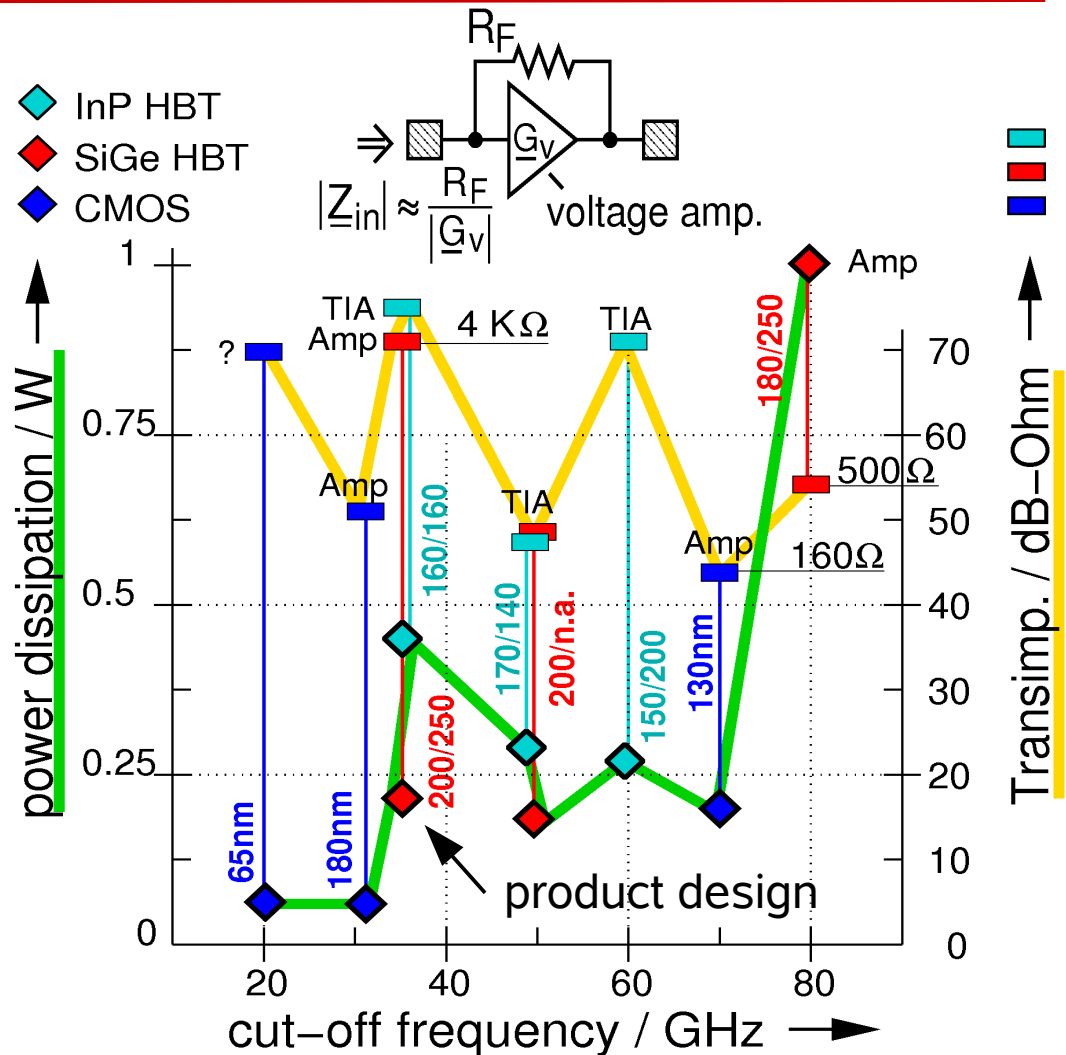
- Higher speed: parasit. $C \downarrow$
- Distributed amp. concept
 - L compensates for C
 - but HBTs input impedance is not pure C
- Emitter degeneration
 - input impedance $\rightarrow C$
 - linearizes
 - gain \downarrow but $\times 2$ is suffic.
- Next. gen. SiGe HBTs:
 - $BV_{CEO} \rightarrow 1\text{ V}$, but ...
 - push-pull $> 2V_{pp}$ @ 40GHz

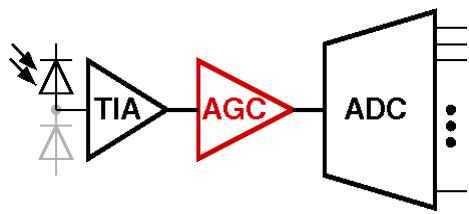




(Transimpedance) Amplifier

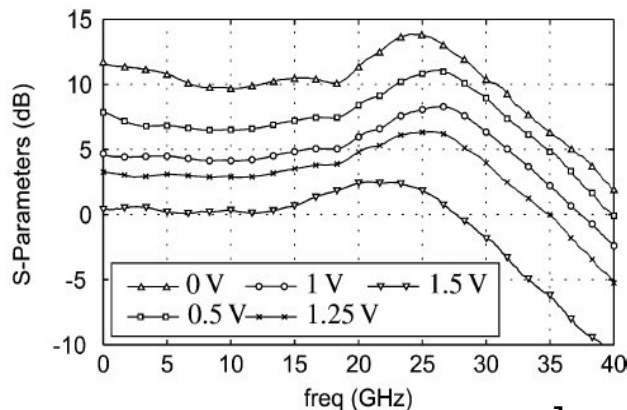
- Parallel feedback (R_F):
 - low ohmic Z_{in}
 - linearization
- Volt. amp. must have $\text{mag}(\underline{G}_V) \uparrow + \text{phase}(\underline{G}_V) \downarrow \rightarrow \text{HBTs } (g_m \uparrow)$
- Parasitics for $f \uparrow$:
 $Z_{in} \rightarrow 50 \Omega$ (34 dB Ω)
- Use 50- Ω pre-amp. w/o feedback \leftrightarrow noise



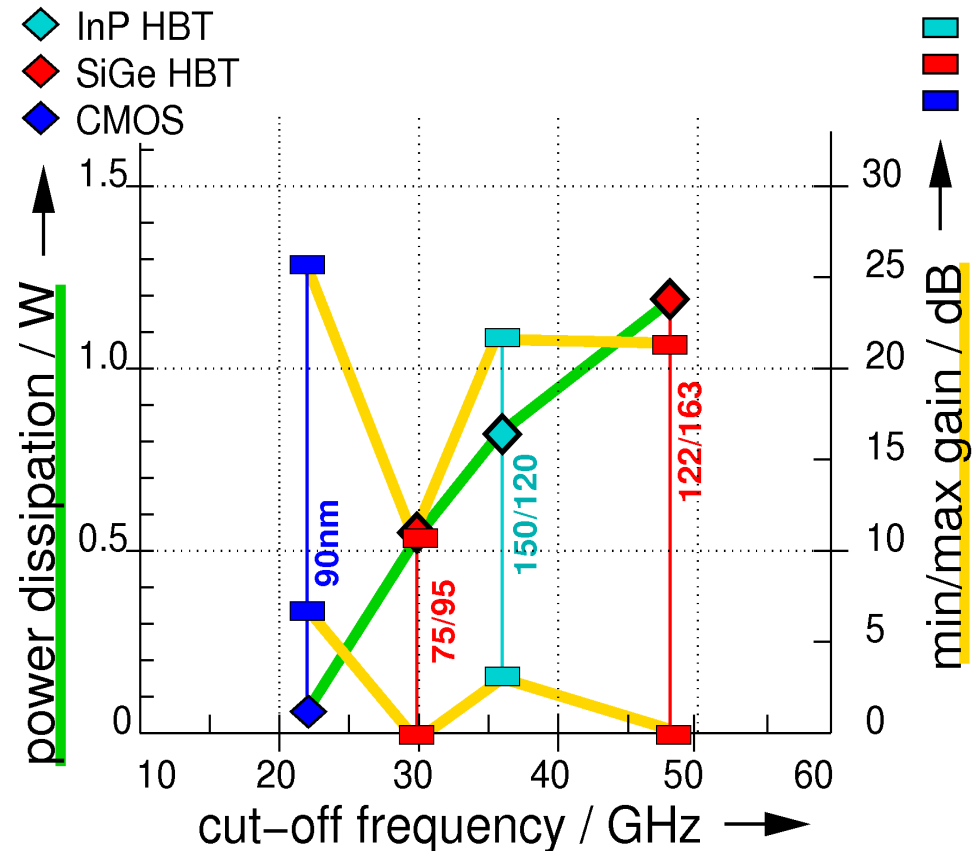


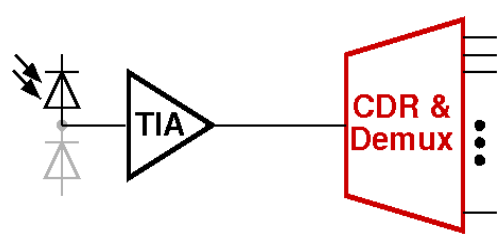
Autom. Gain Control (AGC) Amp

- How to get $P \downarrow$?
 - next SiGe tech. is 3x faster
 - integrate with ADC
 - saves 50- Ω I/O
 - digital peak detect.
- $f_{\text{intens}} \ll f_{\text{AGC}} \ll \min(f_{\text{sig}})$?
- DSP task: gain dependency?



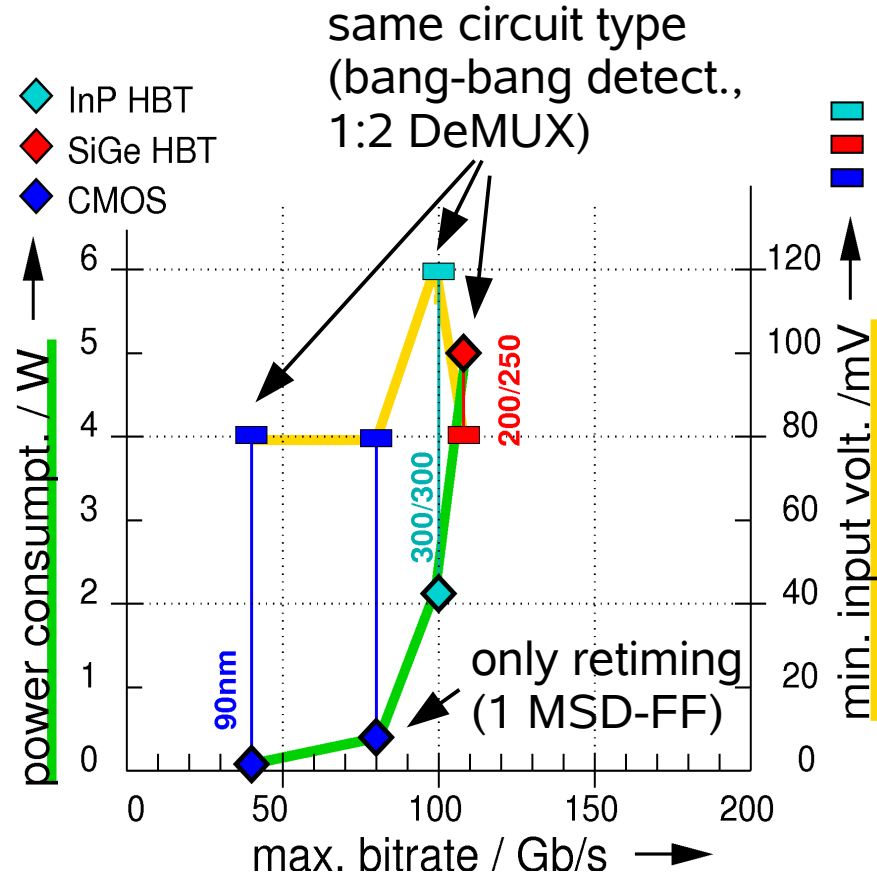
source: Sewiolo et.al [45]

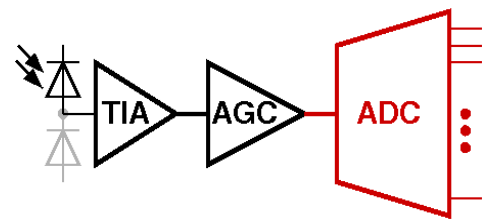




OOK: CDR & DeMUX

- Marginal 112 Gb/s performance
→ High power consumption (2..5 W)
- Improvements by
 - next gen. HBT technol. ($f_t/f_{\max} \approx 300 / 500$ GHz)
 - “novel” circuit concepts
- “Novel”:
 - don't squeeze out bipolar transistor performance ($g_m \uparrow \rightarrow$ operating currents \uparrow)
 - Look how CMOS copes with it's inherent worse g_m !

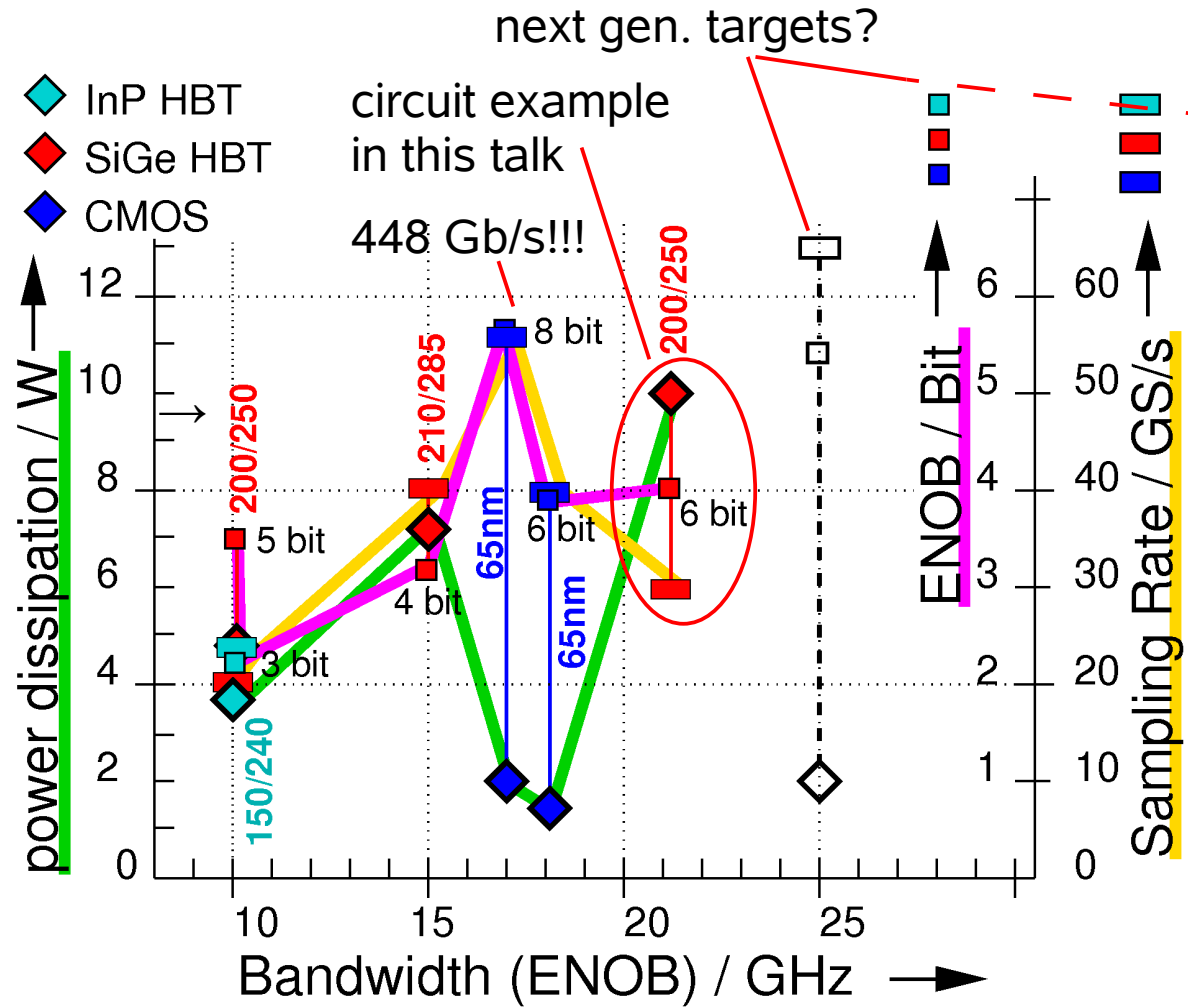




Analog RX: ADC

	CMOS	SiGe
sampl. rate	+	+
ENOB	+	-
power diss.	++	---
bandwidth	-	+
DSP noise	-	+
tech. outlook	-/0	+

- Next generation
 - 60/120 GS/s,
 - ENOB > 5/4
 - BW > 25/50 GHz
 - P = 2 W ?
- DSP < 45 nm

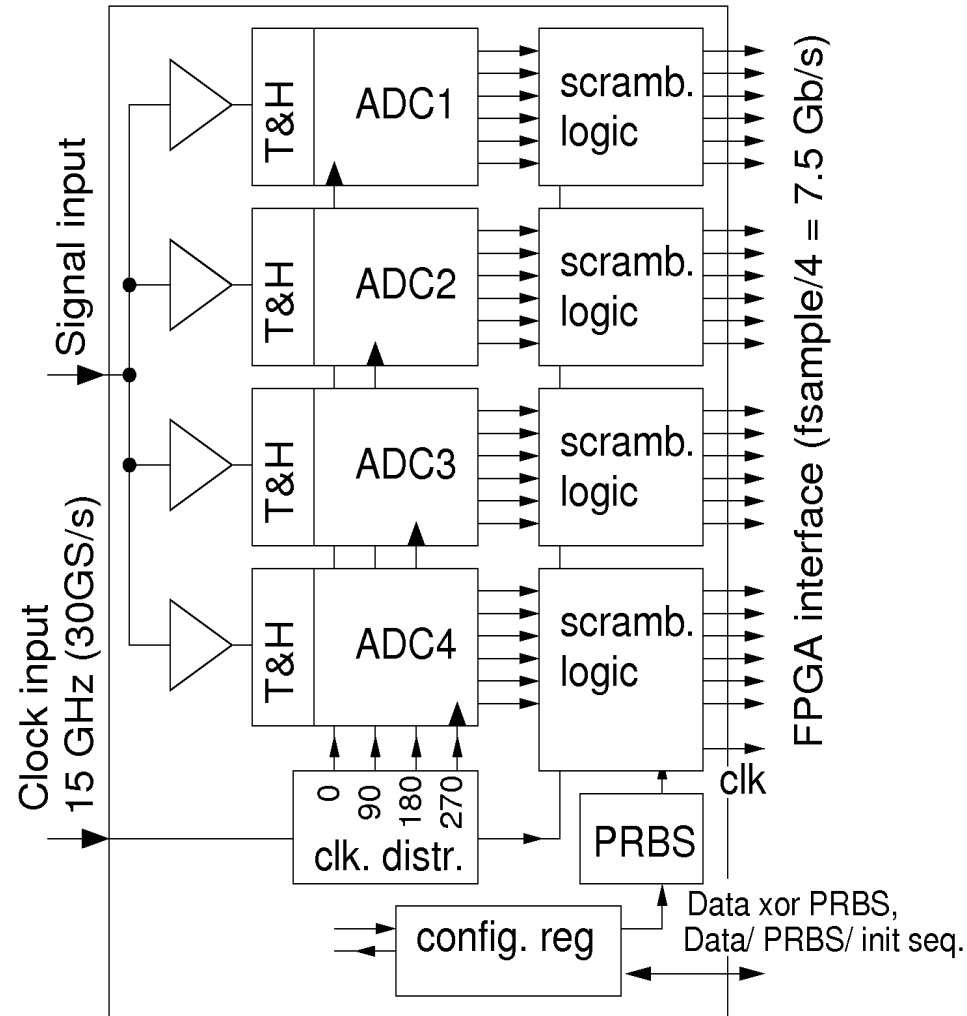


SiGe HBT DAC / ADC demonstrators

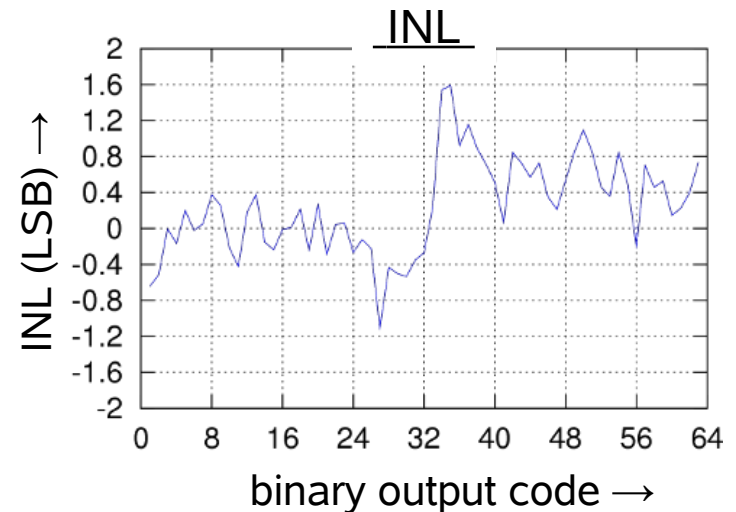
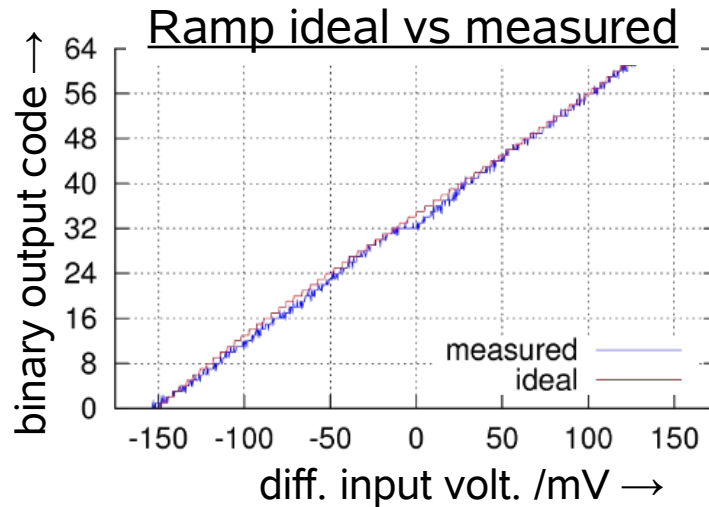
- Part of European 100GET R&D program to
 - evaluate pros, cons and future potential of SiGe converters
 - main target: maximum bandwidth
 - enable system design and transmission experiments
 - main target: real time operation
- Real time interface to commercially available FPGAs
 - Xilinx Virtex 4/5: 24 Transceivers up to 6.5 Gb/s
 - Altera Stratix 4: 24 ... 48 Transceivers up to 8.5 Gb/s
- 6 bit resolution; 4 times multiplexed interface = 24 lanes
 - Virtex4/5: 26 GS/s (+ overclocking)
 - Stratix 4: 34 GS/s

30 GS/s 6 bit ADC demonstrator

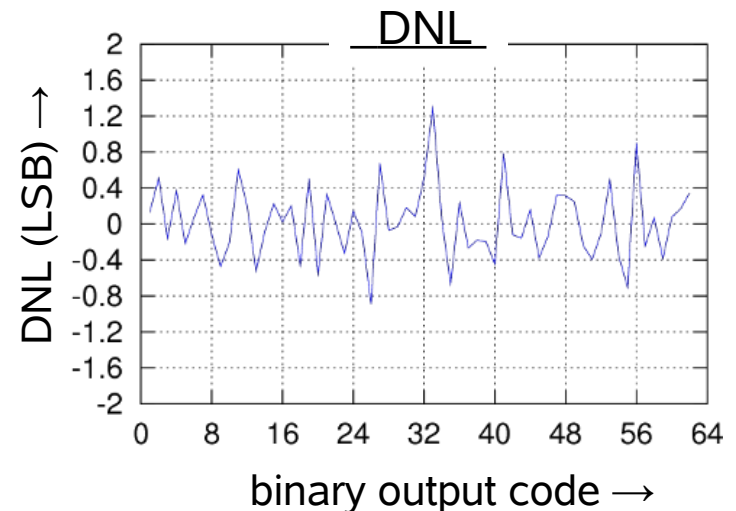
- Transparent sampling 0-30 GS/s
→ scalable: trade speed against power
- Differential or single-ended operation and ac-coupling possible
- 282 mV_{pp} full-scale input
- Input bandwidth \approx 22 GHz
- On-chip 100 ps clock phase shifter
 - Sampling point adjustment
 - Interleaving of 4x 30GS/s ADCs
- Pure SiGe HBT cell based design
 f_T/f_{max} , 200/250 GHz.



ADC static performance

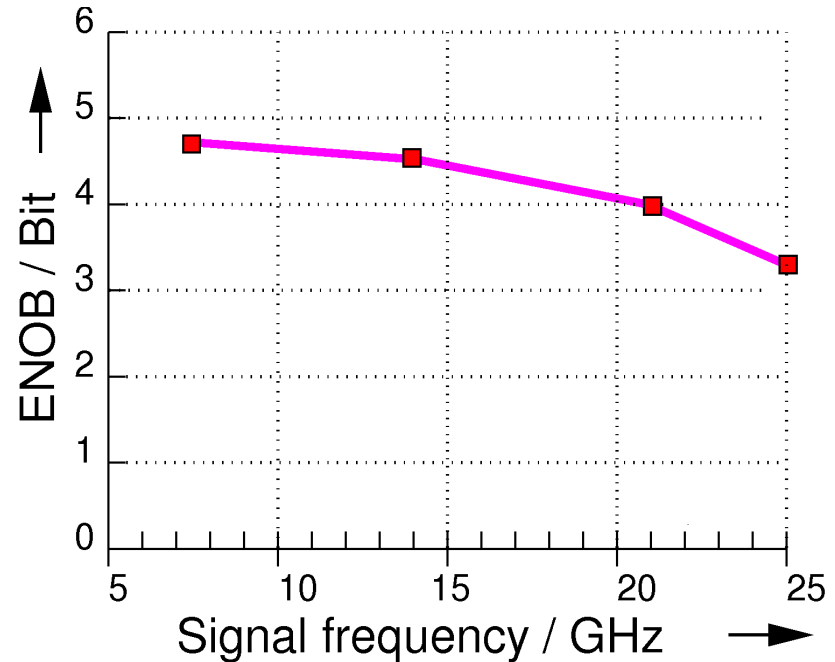


- Optimization of automatic calibration currently in progress:
 - to adjust threshold, offset, and gain of converter stages



ADC dynamic performance

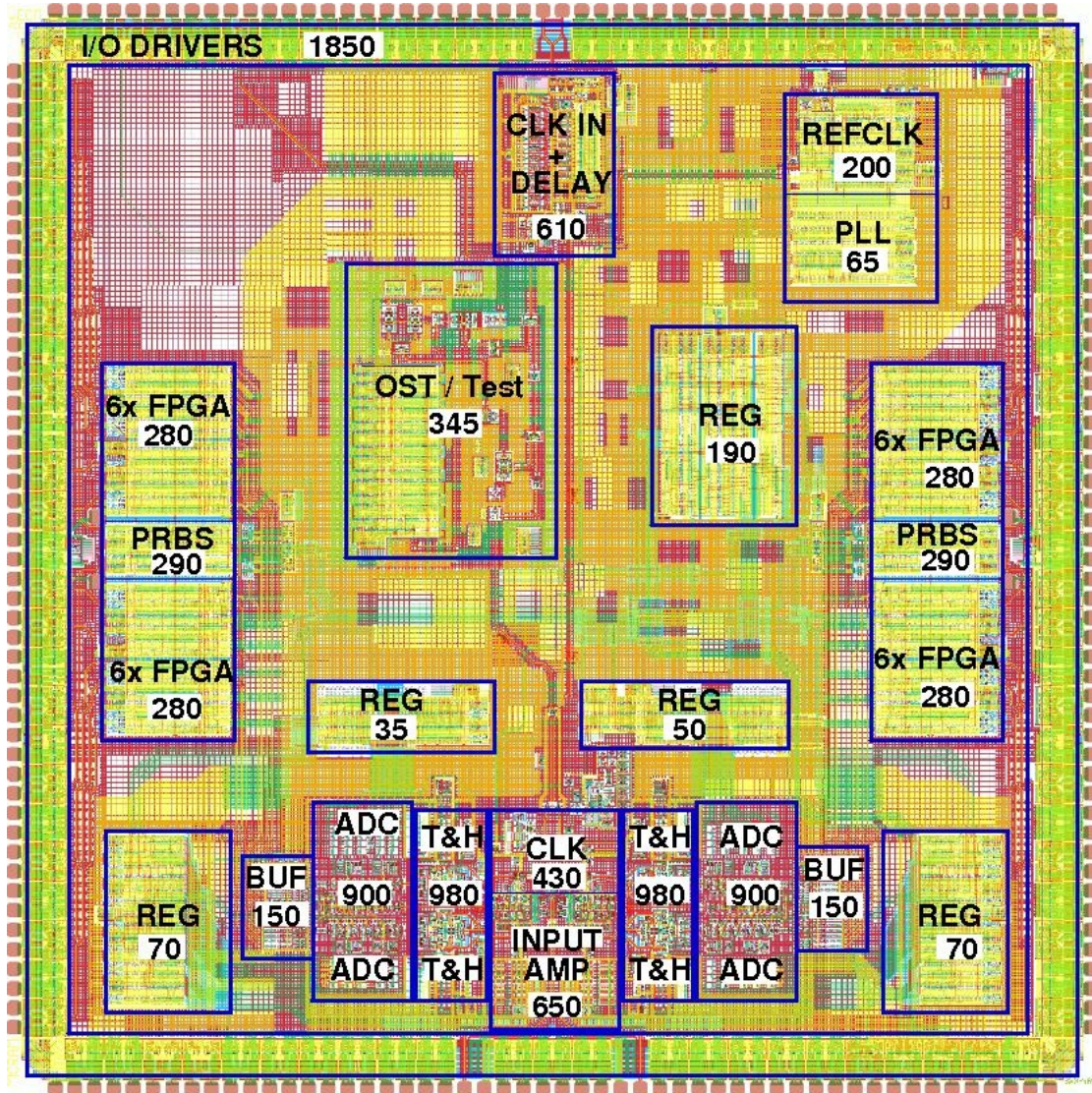
- Measurement: $SR=30$ GS/s
- ENOB estimate based on only 16 samples
- Measurement with internal RC-Oscillator (noise)



- Design issue: ringing of ADC output drivers to FPGA
- Max. interface rate limits sampling rate to 18 GS/s
- Workaround: store 16 samples to internal memory → transfer data via serial low speed register interface to PC → calculate sine-fit (IEEE-STD-1241)

ADC power dissipation map

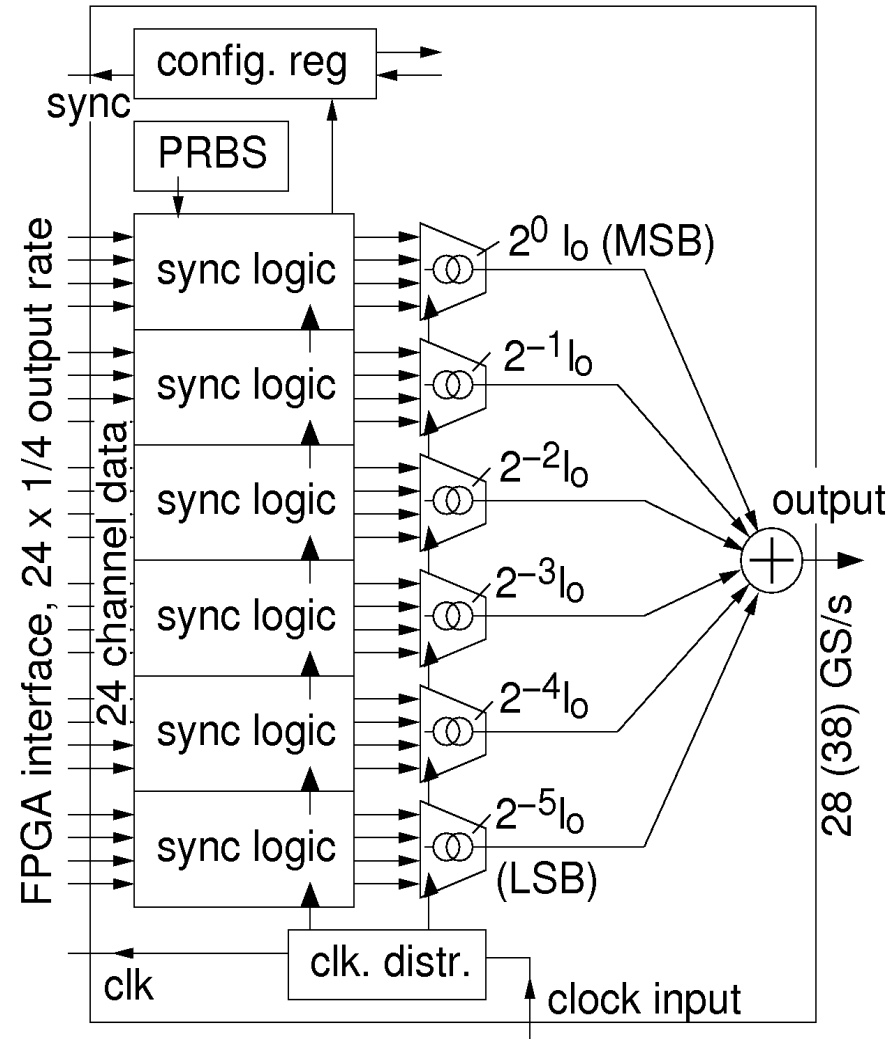
- 10.0 W total power diss.
- ADC core power:
 - 0.65 W input amp
 - 1.96 W T&H
 - 0.43 W Clock
 - 1.80 W ADC
 - 4.84 W
- Logistics + auxiliary:
 - 4.16 W FPGA I/O
 - 1.16 W Aux.
- Savings:
 - safety margins
 - circuit concepts
 - next Bi+CMOS gener.
- Target: 4 W (65 GS/s, 25 GHz BW, 5 ENOB)



⁵Power in highlighted areas (mW), chip size 5x5 mm²

30 (38) GS/s 6 bit DAC demonstrator

- CML output, on-chip 50- Ω term.
- Full-scale output programmable:
0.25 ... 0.9 mV_{pp} (single ended)
0.50 ... 1.8 V_{pp} (differential).
- Bandwidth: > 25 GHz.
- Speed limit at 28 GS/s
(7 Gb/s overclocked Virtex 4 I/Os)
- 38 GS/s core speed
(but timing issue to be solved)
- Pure SiGe HBT cell based design
 f_T/f_{max} , 200/250 GHz.



DAC power dissipation map

If all blocks powered on:

8.4 W FPGA I/O+Sync.

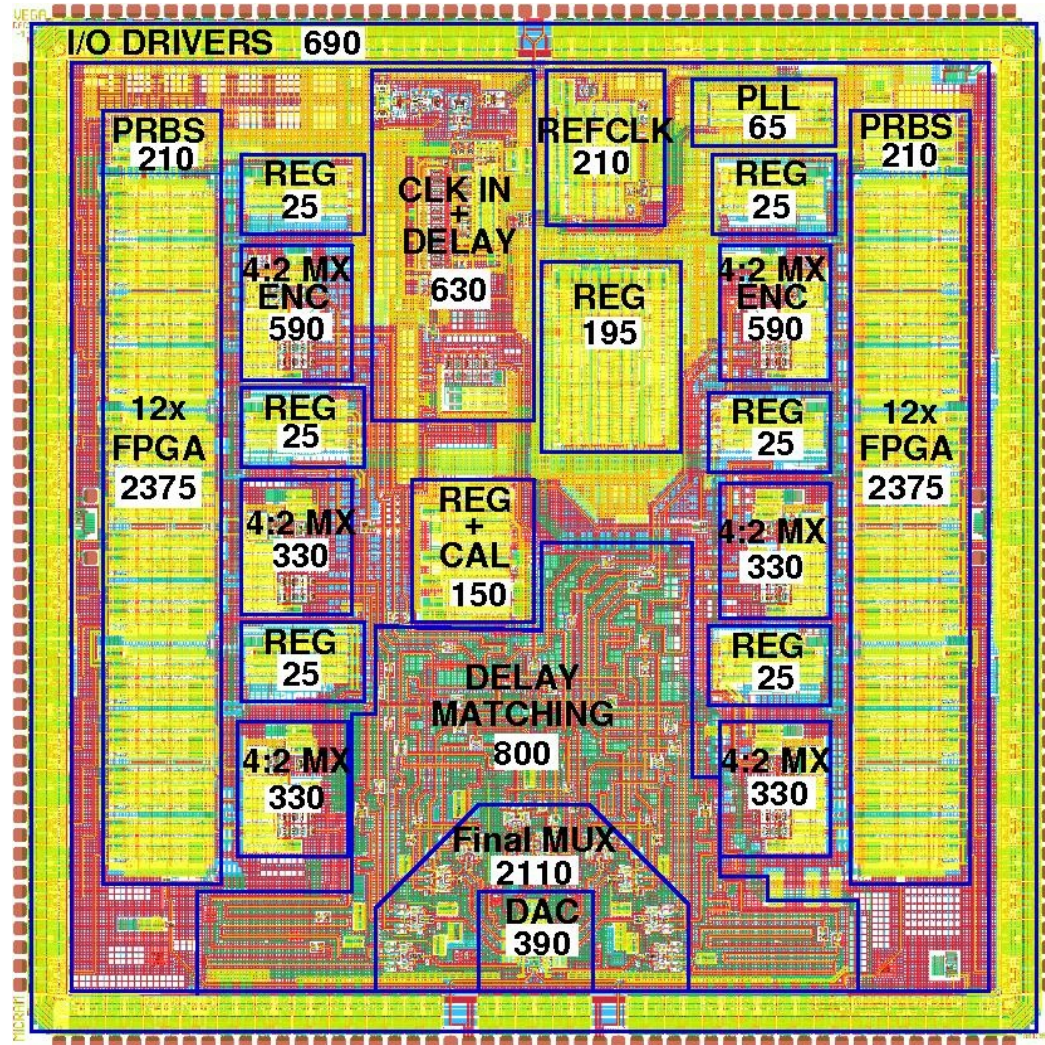
1.3 W Regs., cal, ...

3.3 W High speed circ.

13.0 W Total

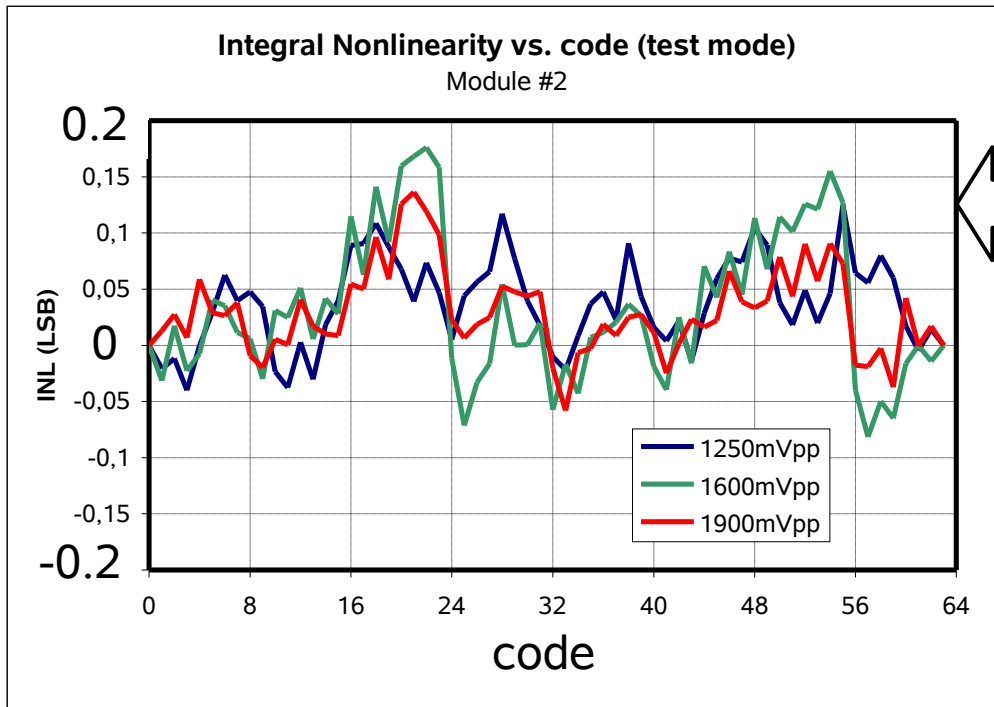
High speed consumes
„only“ $\frac{1}{4}$ of total power

$\frac{3}{4}$ of total power
due to „logistics“
at 7.5...15 Gb/s.



Power in highlighted areas (mW), chip size 5x5 mm²

DAC performance



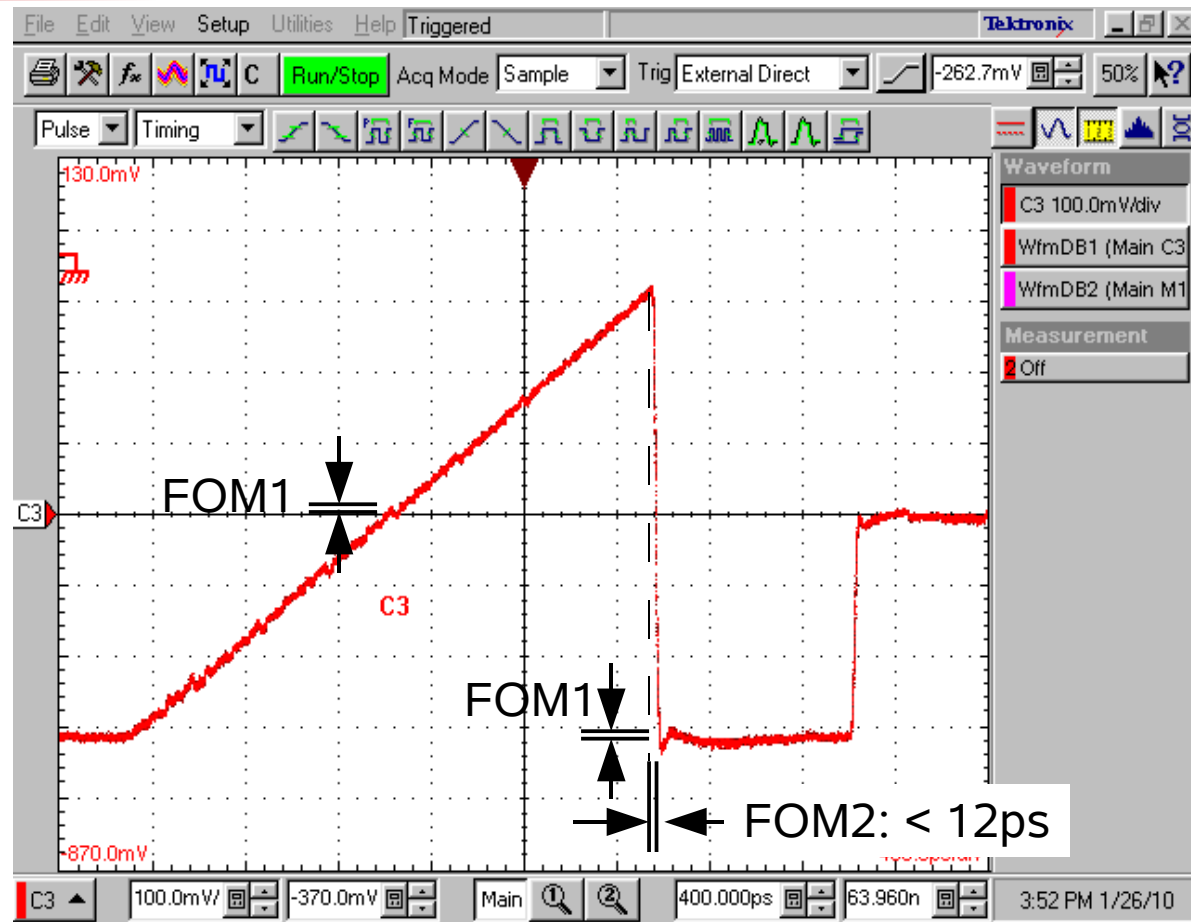
- INL measurement
- DC Ramp
- DAC running at 30 GS/s
- Code applied via internal register
- 50- Ω DC termination

- Dynamic FOMs @ 28GS/s measured up to
 - Nyquist freq. (14 GHz)
 - full meas. BW (26.5 GHz)

	DAC @ 28 GS/s			
	875 MHz		218.75 MHz	
	0-26 GHz	0-14 GHz	0-26 GHz	0-14 GHz
SINAD [dB]	31,11	33,49	34,98	36,82
ENOB [bit]	4,88	5,27	5,52	5,82
SFDR [dB]	42,60	36,97	45,79	47,74
SNR [dB]	41,48	44,30	41,74	44,43
THD [dB]	-31,53	-33,86	-36,01	-37,64

DAC transient performance

- FOM 1: glitches
 - MSB-1 ↔ MSB
 - all along a ramp
 - step response (over/undershoot)
 - shall be $< \pm \frac{1}{2}$ LSB
- FOM 2: rise/fall time
 - full scale step
 - shall reach $\pm \frac{1}{2}$ LSB of start and end values
- Is this really required?



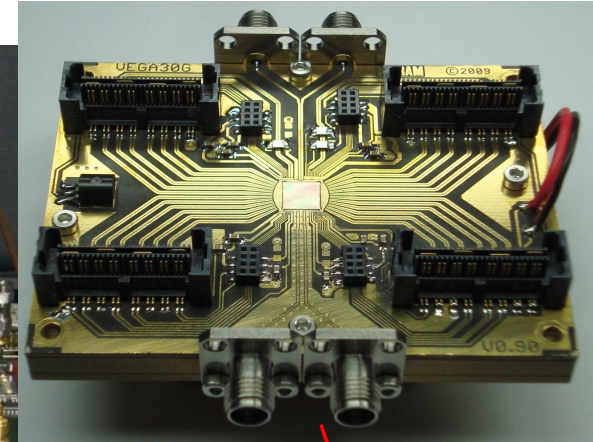
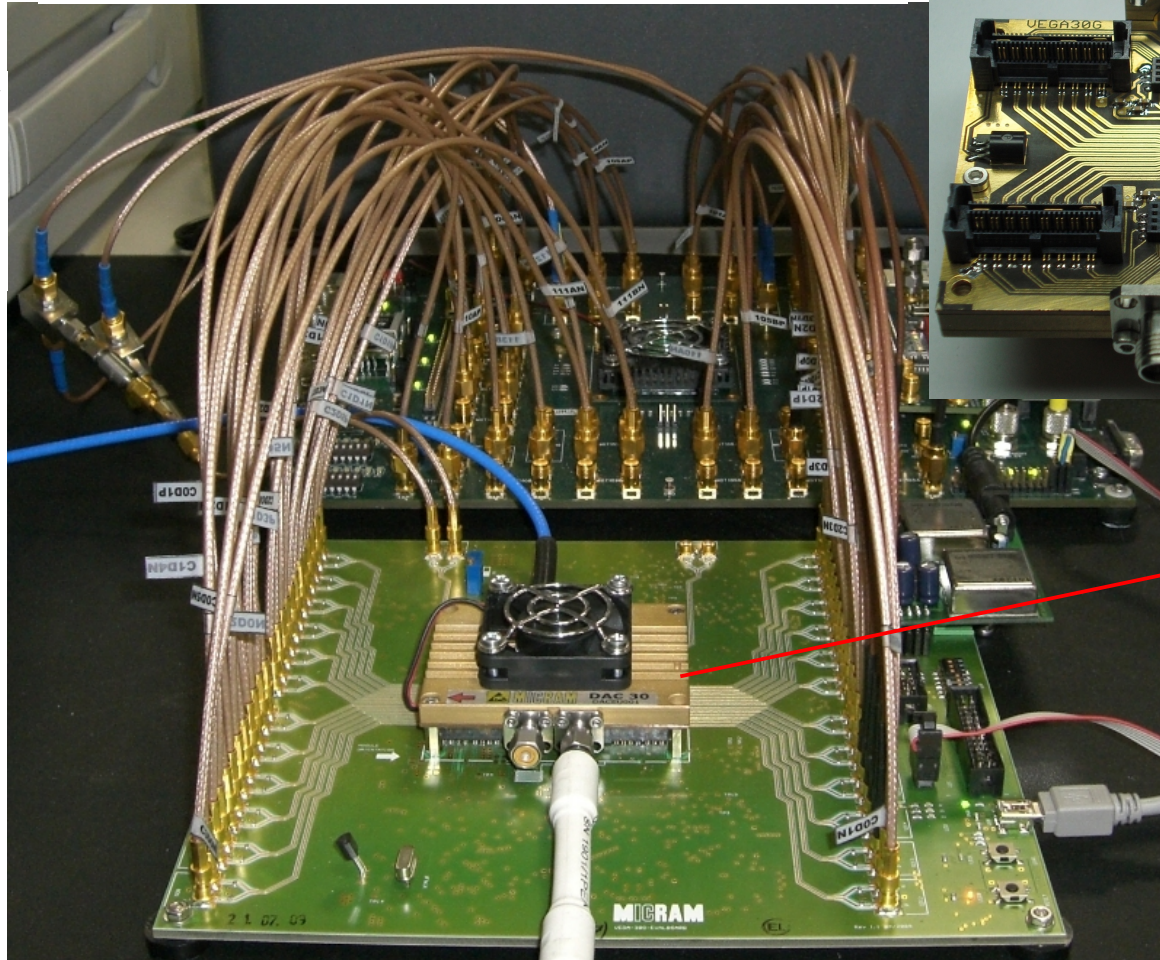
ADC/DAC boards for real time experiments

Xilinx ML424 Board with Virtex4-FX140

48 RF-cables for
24 differential
SerDes links

15 GHz Clock →
input

Reference clock
(:40) for FPGA is
generated by
the DAC

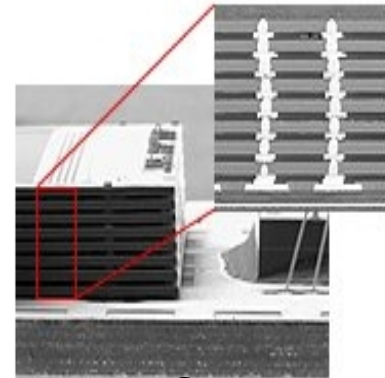


DAC module

30 GS/s output

Outlook on high-speed electronics

- Rethink transceiver partitioning: combine, relax and release functions/tasks and performance
 - direct MZM drive, integrate AGC, adaptive DAC step size ...
 - DSP algorith. to consider electronics as a part of the channel
- Next generation BiCMOS technology: speed x2
 - trade speed against power efficiency
 - novel concepts to replace g_m -driven performance
- SiP: no need for low-ohmic 50- Ω TML interfaces
 - Use simple + high ohmic, high-speed interfaces
- 3-D TSV interconnects becomes cheap Si standard assembly (DRAM, MEMS). Tend: 2000 I/Os, $\varnothing=2\mu\text{m}$, $l=20\mu\text{m}$
 - combine best CMOS and SiGe technologies \rightarrow Bi+CMOS



source: Samsung