High-Speed Electronic Circuits for 100 Gb/s Transport Networks

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	MUX					CDR&Demux				
	BR/ Gb/s	V_{out} /mV_{pp}	P/ W	type, f_t/f_{max} /GHz	Ref.	BR/ Gb/s	V_{min}/ V	P/ mW	type, f_t/f_{max} /GHz	Ref.
III-V HBT (InP)	165 100	400 700	1.6 0.8	4:1, >300/300 speed/power trade-off	[46]	100	120	2100	1:2, > 300/300	[8]
SiGe HBT, BiCMOS	132 86	500 600	1.45 0.85	4:1, 210/n.a. 8:1, 150/150	[47] [3]	107	80	5000	1:2, 180/200	[10]
CMOS	60 50 40 40 40	100 200 400 560 800	0.01 0.1 0.13 0.33 2.8	2:1 selector, 90nm 2:1, 130nm 4:1ext. clk, 90nm 4:1& intl.CMU, 90nm 16:1 SFI-5, 65nm	[4] [5] [6] [7] [13]	81 40 40 40 40	80 n.a. n.a. n.a. n.a.	200 57 48 2800	TIA & full-rate latch, 65nm 1:1 CDR (retimer), 90nm 1:2, 90nm 1:16 SFI-5, 65nm	[11] [12] [30] [13]

Bitrate (BR), differential outp. volt. (V_{out}), power (P), transistor transit / maximum oscillation frequency (f_t/f_{max}), min. input voltage (V_{min}).

	Driver					TIA					AGC				
	BR/BW Gb/s/GHz	V_{max}/G/type /V_{pp}/dB/ -	P / W	f_t/f_{max} / GHZ	Ref.	BR/BW / Gb/s/GHz	Z_{TI} / dBΩ	P / mW	f_t/f_{max} / GHZ	Ref.	BW/ GHz	G_{max}/G_{min} /dB	P / mW	f_t/f_{max} / GHZ	Ref.
III-V HBT (InP)	100/120 n.a./110 40/50	2.3/21 /ds 2.8/17 /ds 11.3/25 /dd	0.61 0.22 3.0	350/370 337/345 150/200	[15] [16] [17]	40/60 43/35 40/49	71 75 48	271 450 286	150/200 160/160 170/140.	[23] [24] [25]	36	22/3	814	150/120	[32]
SiGe HBT	40/32 40/22 50/n.a.	2.5/13 /dd 7.2[1]/42 /dd 2.0/Pmux	0.23 3.6 2.0	80/90 160/160 72/75	[18] [19] [14]	84/80 56/35 40/50	54 72 49	1W 211 182	180/250 200/250 200/n.a.	[26] [27] [25]	48 30	21.5/0 11/0	1200[3] 560	122/163 75/95	[33] [45]
CMOS	n.a./80 40/33.4 40/39.4 n.a./90	n.a./7.4 /ds 1.6/16 /ds 1.3/20 /ds 2.5/11 /ds	0.12 0.26 0.25 0.21	90nm 180nm " 120nm SOI	[20] [21] " [22]	n.a./70 40/31 40/22 25/20	44 51 66 70	200 60 75[2] 70	130nm 180nm 90nm 65nm	[28] [29] [30] [31]	22	26/7	75	90nm	[30]

Bitrate (BR), bandwidth (BW), driver type distributed differential/single ended (dd/ds), max. differential (dd) /single ended (ds) output voltage swing (V_{max}), gain (G), transimpedance (Z_{TI}), for 50-Ω input: Z_{TI} =voltage gain + 34 dB, max./min. voltage gain (G_{max}/G_{min}), [1] 75Ω driver, [2] TIA and AGC, [3] additional 1.6 W are consumed by a full-wave recifier.

	DAC				ADC			
	SR/Res GS/s / -	t_r/V_{fs} ps/V	P / W	f_t/f_{max}, Ref / GHz / -	SR/f_{ENOB} / GS/s/GHz	Res / ENOB	P / W	f_t/f_{max}, Ref / GHz/ -
III-V HBT	32/6	30/0.3	1.4	175/260, [34]	24/10	3/2.3	3.8[2]	150/240, [39]
SiGe HBT, BiCMOS	34/6 20/8 20/6	<12/1.6 >24[1]/0.8 n.a./1.0	12.5 2.5 0.36	200/250, [35] 190/190, [36] 150/200, [37]	35/8 30/22 40/15 20/10	4/3.2 6/4.0 4/3.2[2] 5/3.5	4.5 10 7.2 4.9	160/n.a., [40] 200/250, [41] 210/285, [49] 200/250, [42]
CMOS	12/8	>31[1]/1.0	0.19	90nm, [38]	56/17 40/18	8/5.68 6/3,9	2 1.5	65nm, [43] 65nm, [44]

Sampling rate (SR), physical resolution (Res), 20%-80% rise/fall-time (t_r) at full-scale swing (V_{fs}), effective number of bits (ENOB) at f =(f_{ENOB}), [1] 0.22/resolution bandwidth, [2] with decoder logic. [3]) simulated, [4] at SR=20 GS/s and f_{ENOB}.=19 GHz an ENOB=3 was measured but at unspecified higer power consumption.

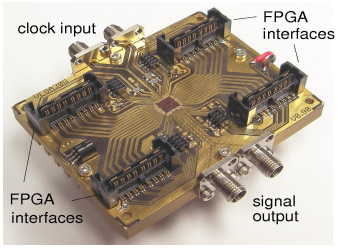

Fig.1. DAC module [35].

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