Exploring the limits:

Development of Integrated High–Speed Circuits

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Fig. 2

40th Anniversary – Moores Law Still Valid

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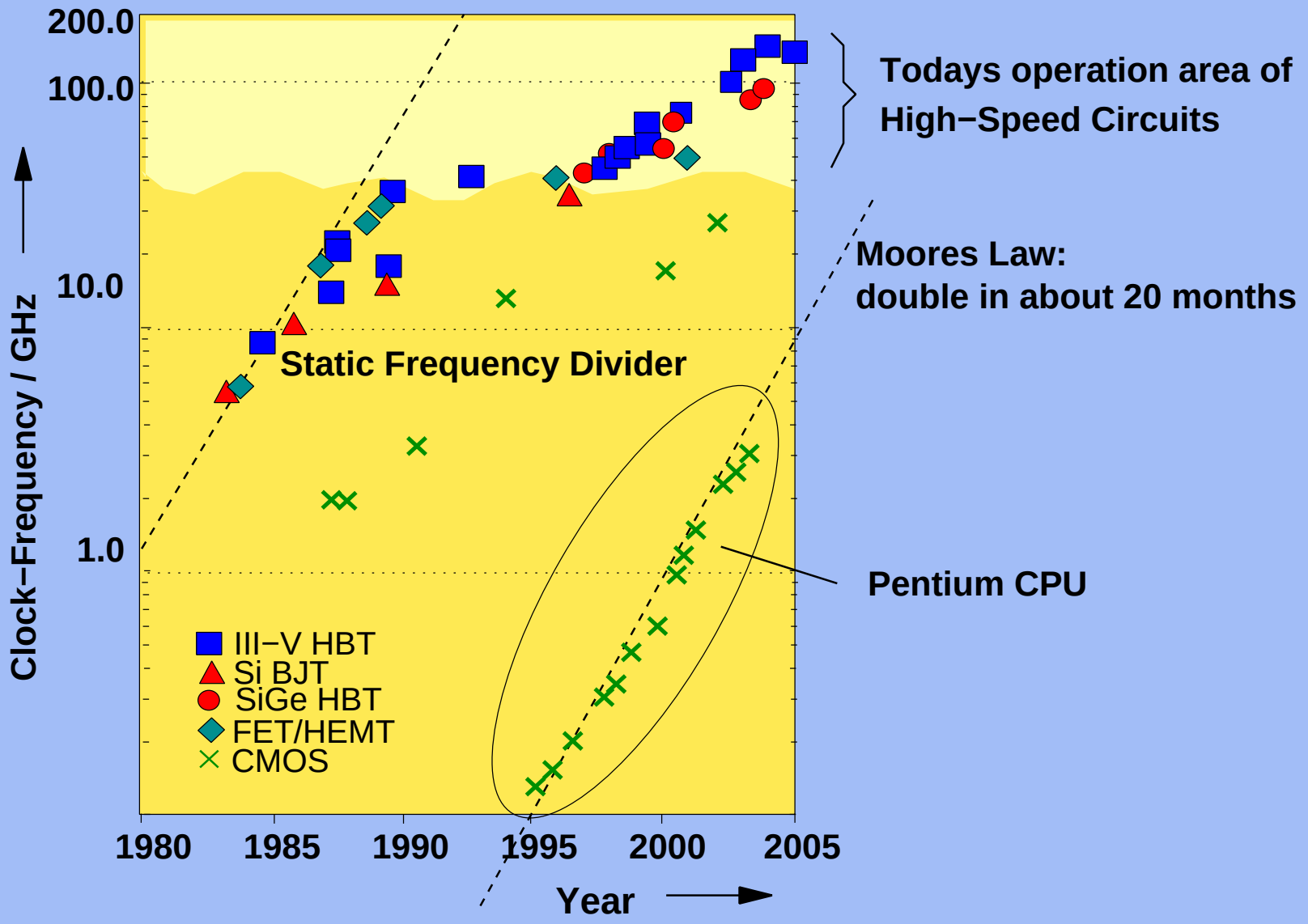

(Why) Does increase in speed slow down?

Fig. 3

Do we need (even) faster Semiconductor–Technologies?

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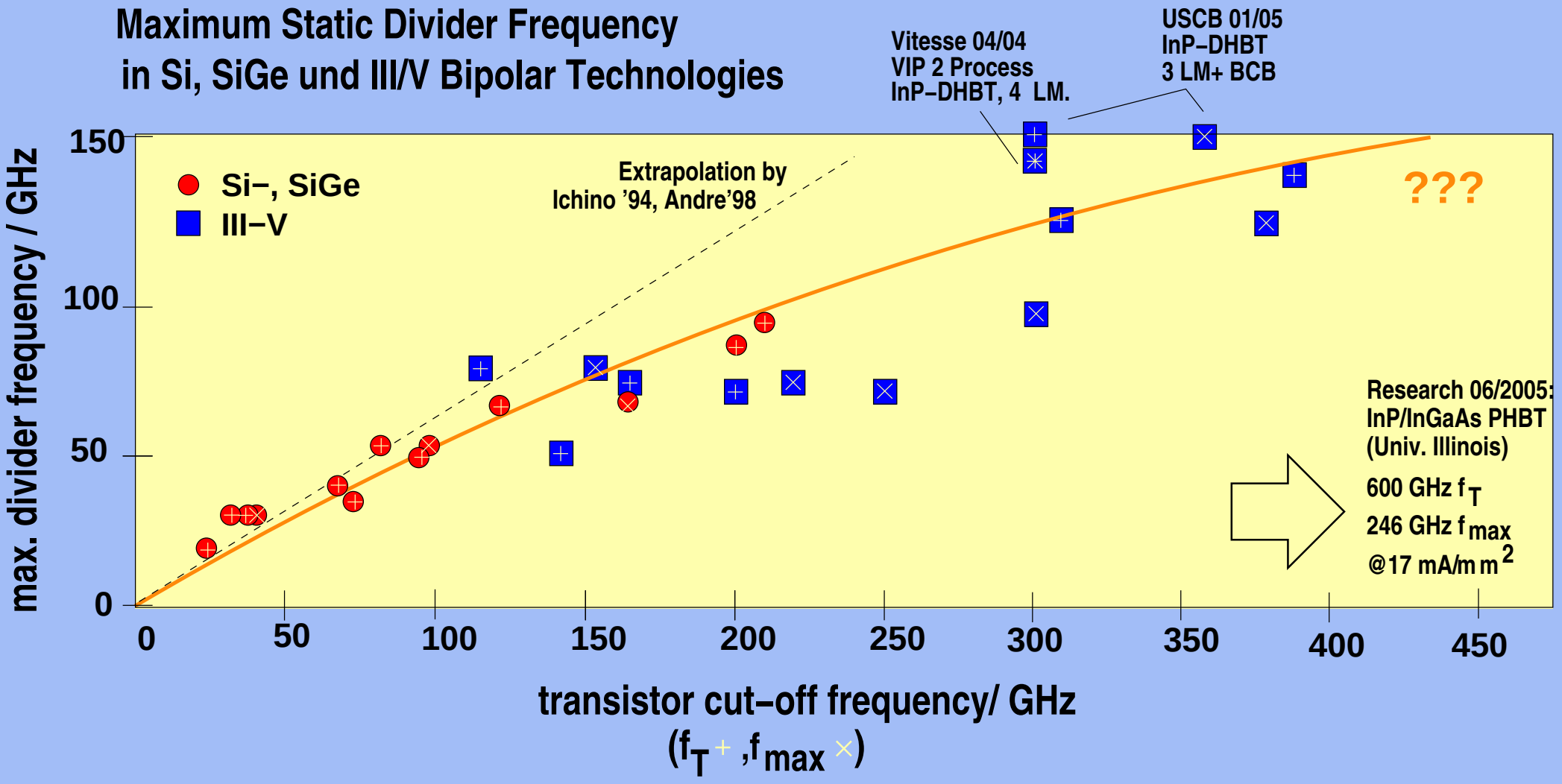

Speed does not scale with transistor cut–off frequency – WHY ?

Fig. 4

Outline: Some Speed–Limiting Factors...

... And Ways to Surpass the Limits.

- How fast is the "intrinsic" transistor?
- Troublesome layout parasitics
- High Mismatch – High–Speed
- Borderline design: Speed–Optimisation
- Chip–Assembly – a multidisciplinary challenge
- Measurement setup – the Chicken and the Egg Dilemma
- Some latest 100 Gbit/s Receiver/Transmitter results

"A rough overview from the circuit designers perspectice"

Fig. 4

What limits bipolar–transistor speed?

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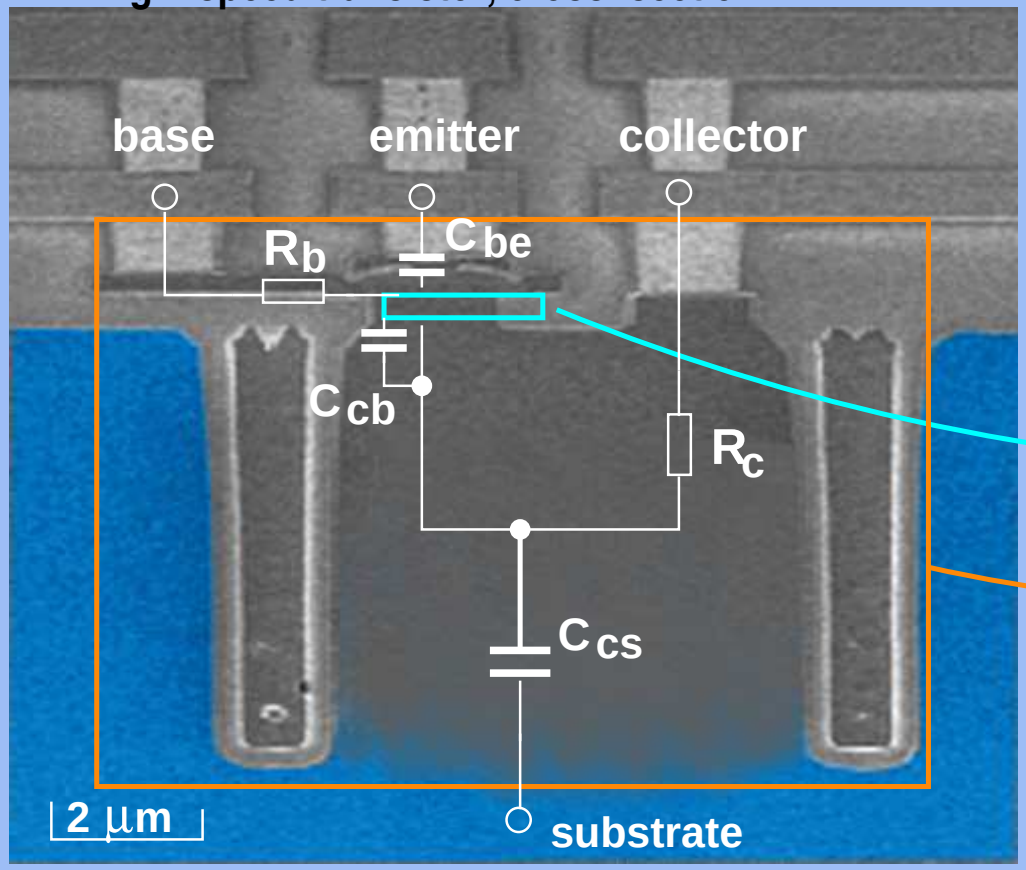
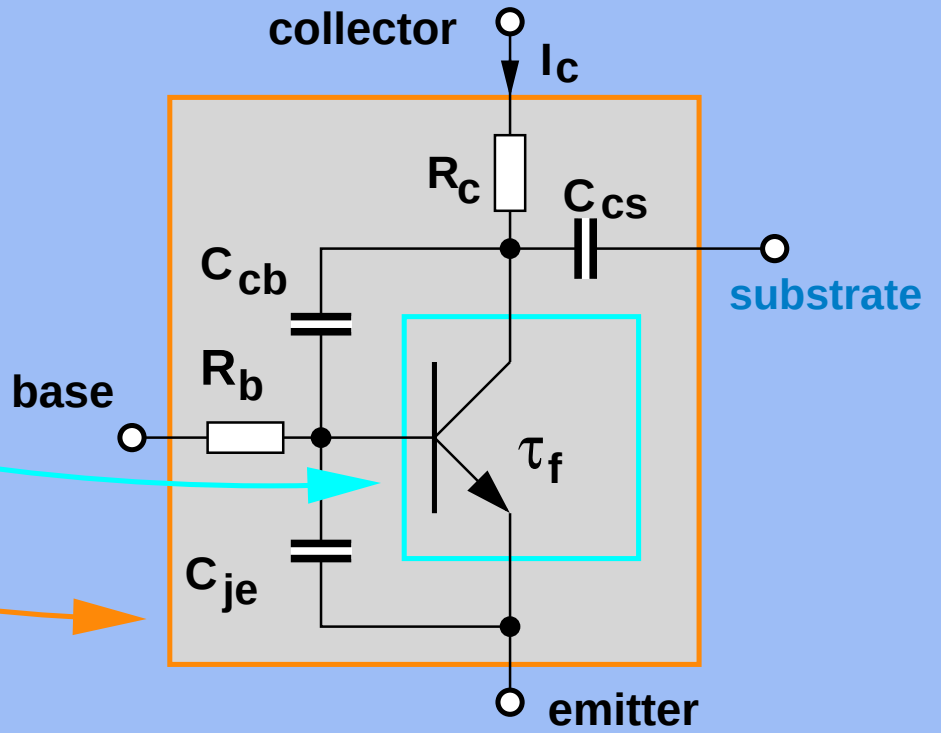
high–speed transistor, cross–section





high cut–off frequencies , f_T f_{max} :

$$f_T \sim \frac{1}{\frac{C_{je}}{I_c} u_T + \tau_f + \ldots}$$

$$f_{max} = \sqrt{\frac{f_T}{8 \pi R_b C_{cb}}}$$

- small R, C, τ ⇨ small transistor size
- high collector currrent I_c

⇨ high current density

Higher Speed ⇨ **Higher Current Density?**

Fig. 6

Parasitic Capacitances of Transistor Metallization

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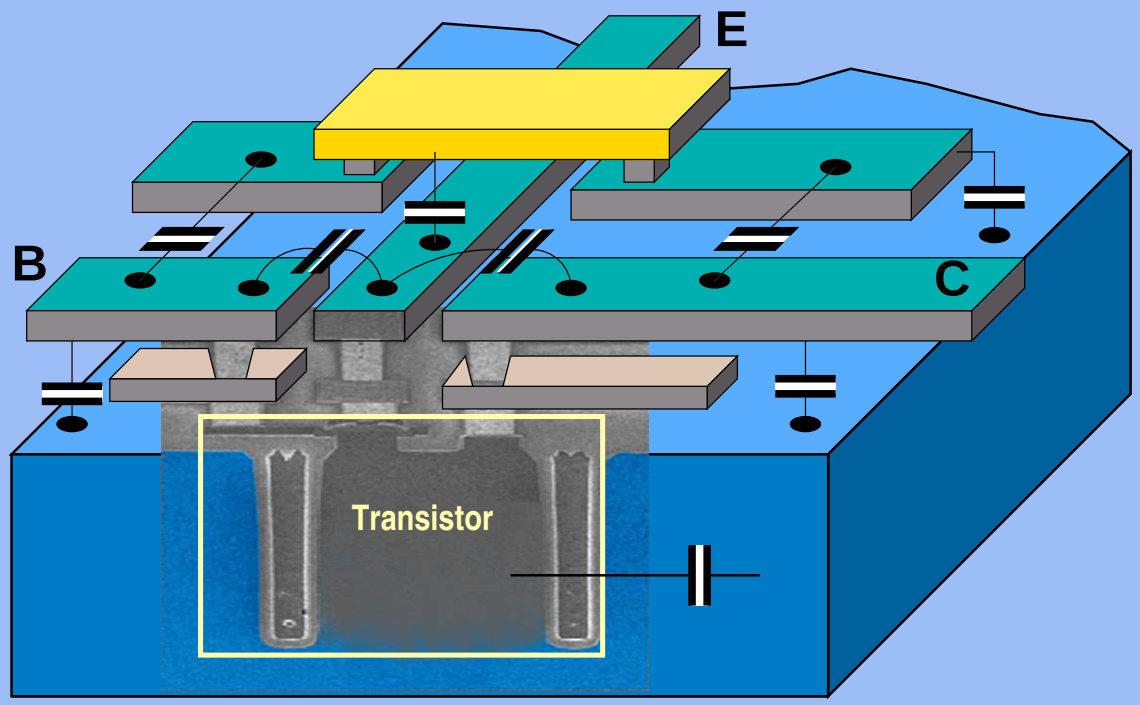
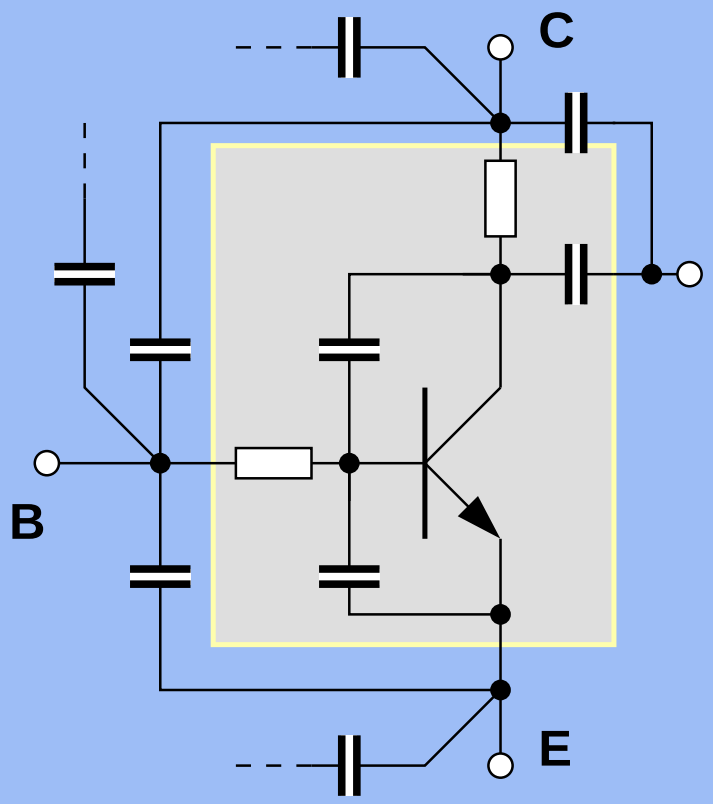


short circuit at increasing frequency:



Electromigration determines minimum metal cross–section area

Capacity reduction by:

- **lower dielectric constant**
- **thicker dielectric**
- **smaller metal width/area (eg. Copper insted of Aluminum)**

Technological limit almost exhausted ⇨ **New Materials/Technology**

Fig. 7

Interconnect Parasitics Dominate Transistor Parasitics

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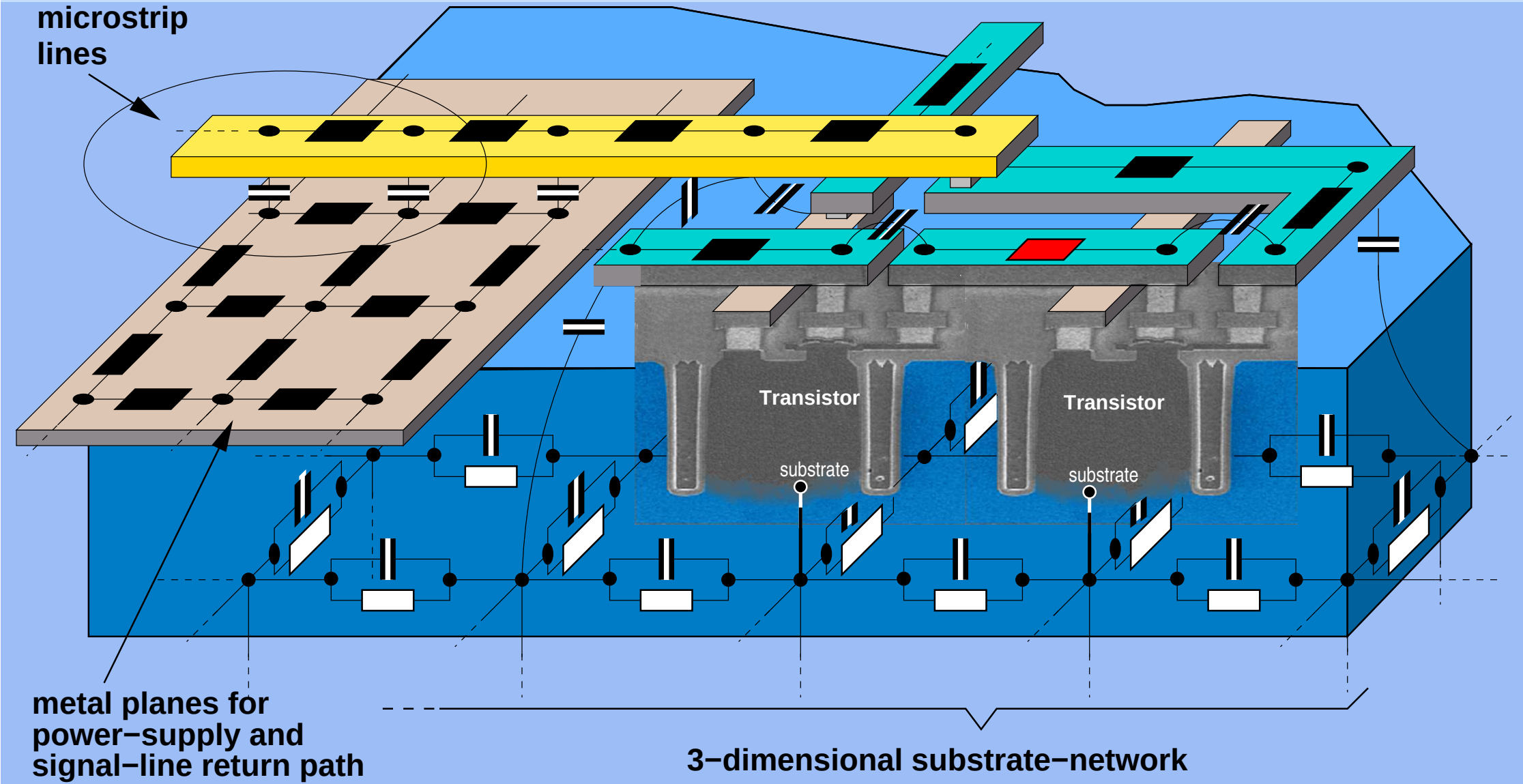

Layout: Very komplex 3–Dim. RLCM Network with major influence on the circuit's speed.

Fig. 8

Layout Determines Speed−Limit

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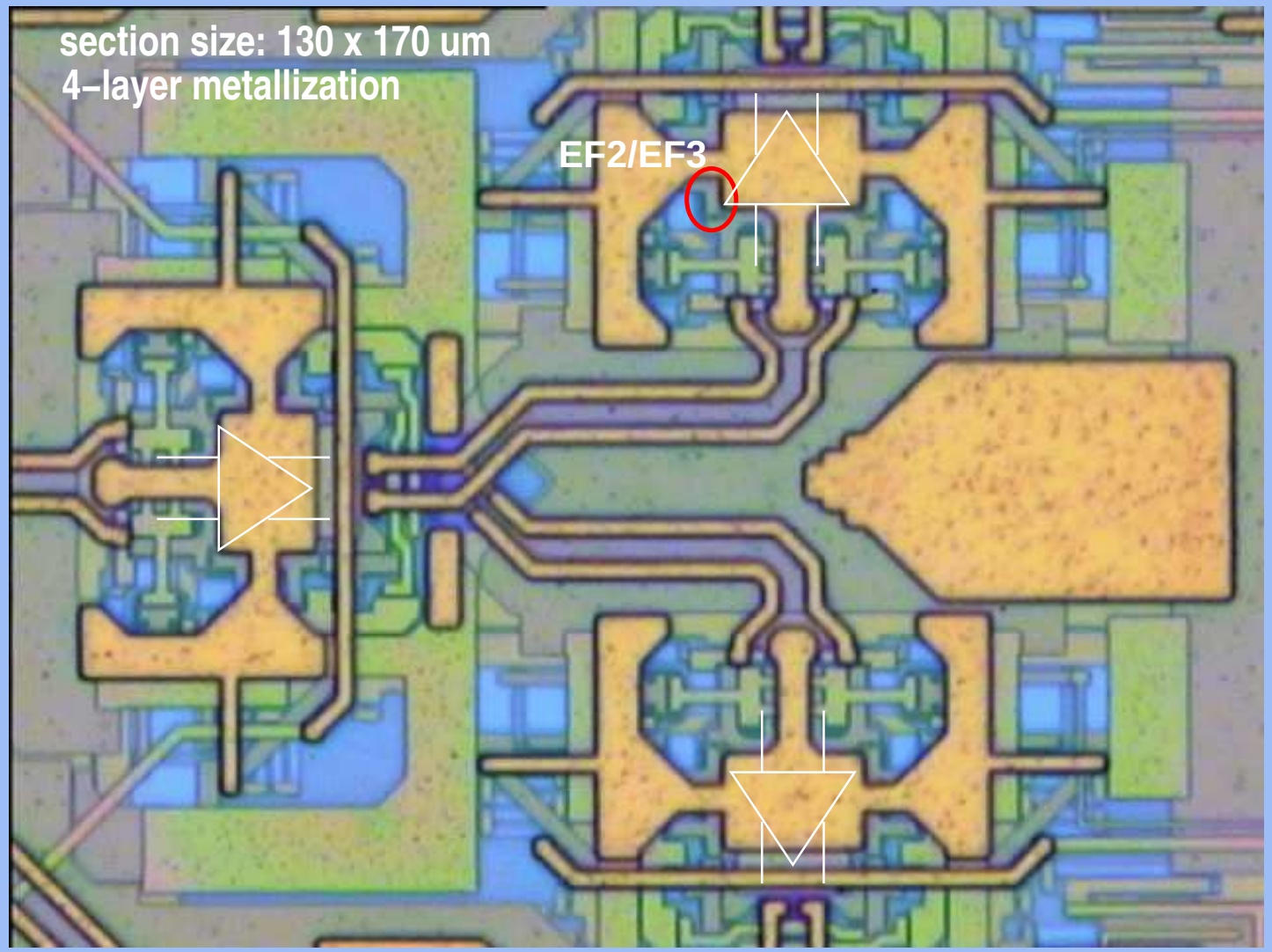
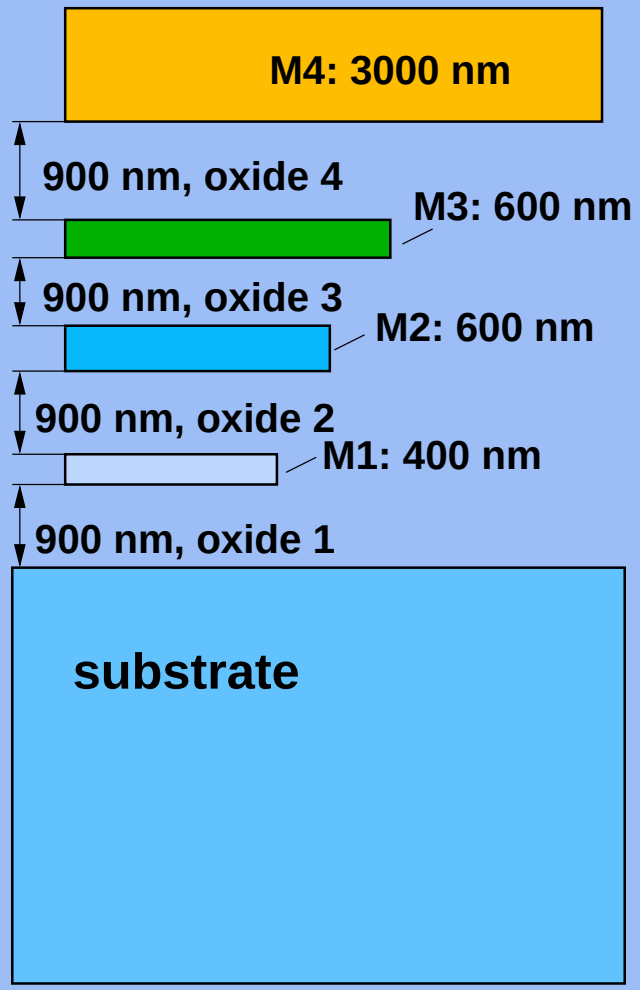
Example: Layout of 1:2 Clock Distribution Amplifier



metal stack:



Small parasitic C: small (tall) wires, thick oxide, low dielectric constant

Small parasitic L: broad wires (tradeoff with C), short wires (often not possible) –> L becomes critical!

Fig. 9

Optimization Goal: Short Wiring

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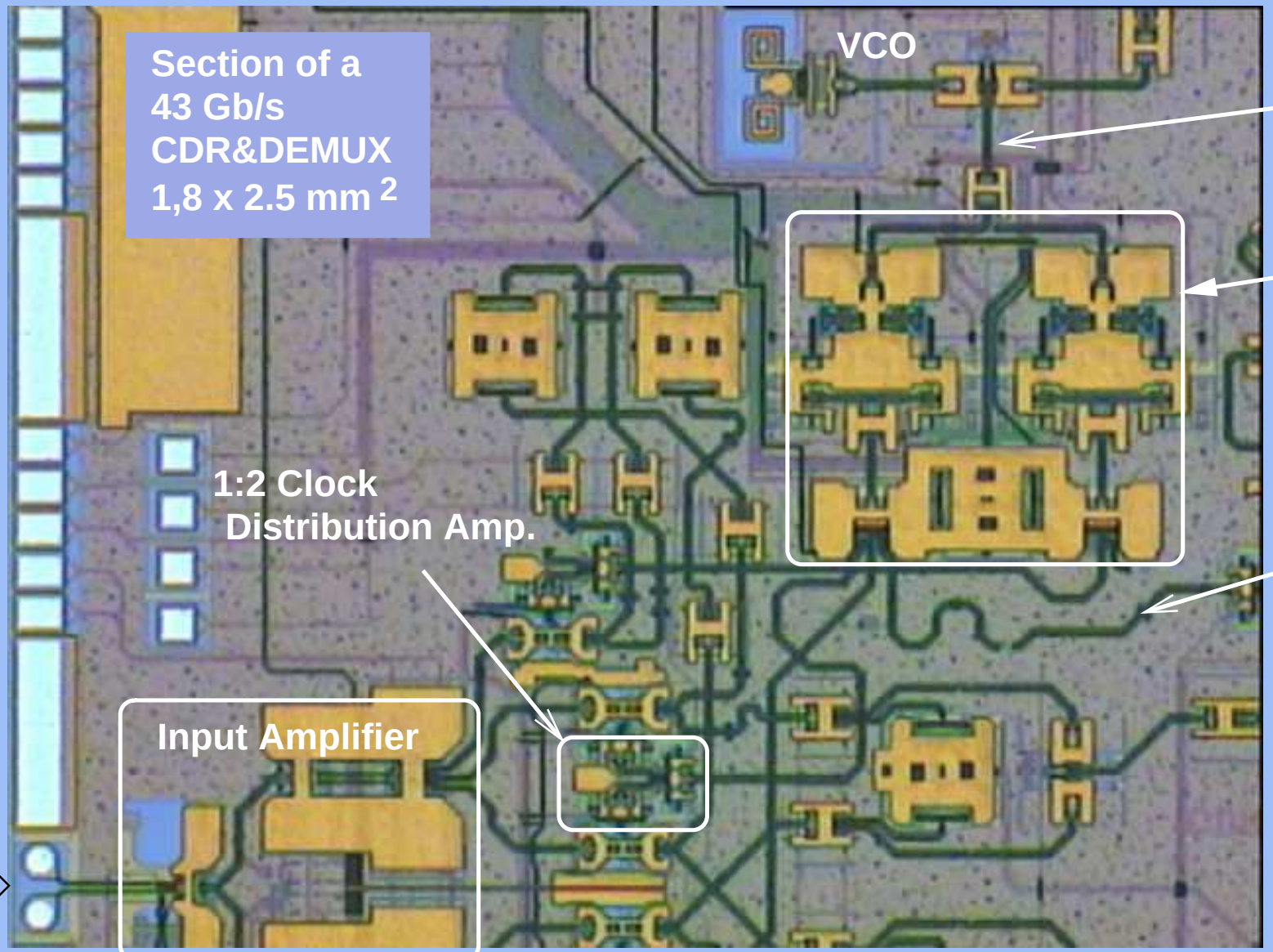

Constraints: Line lengts of dedicated signals must be at the same length

Fig. 10

Design Rules Impact on Speed

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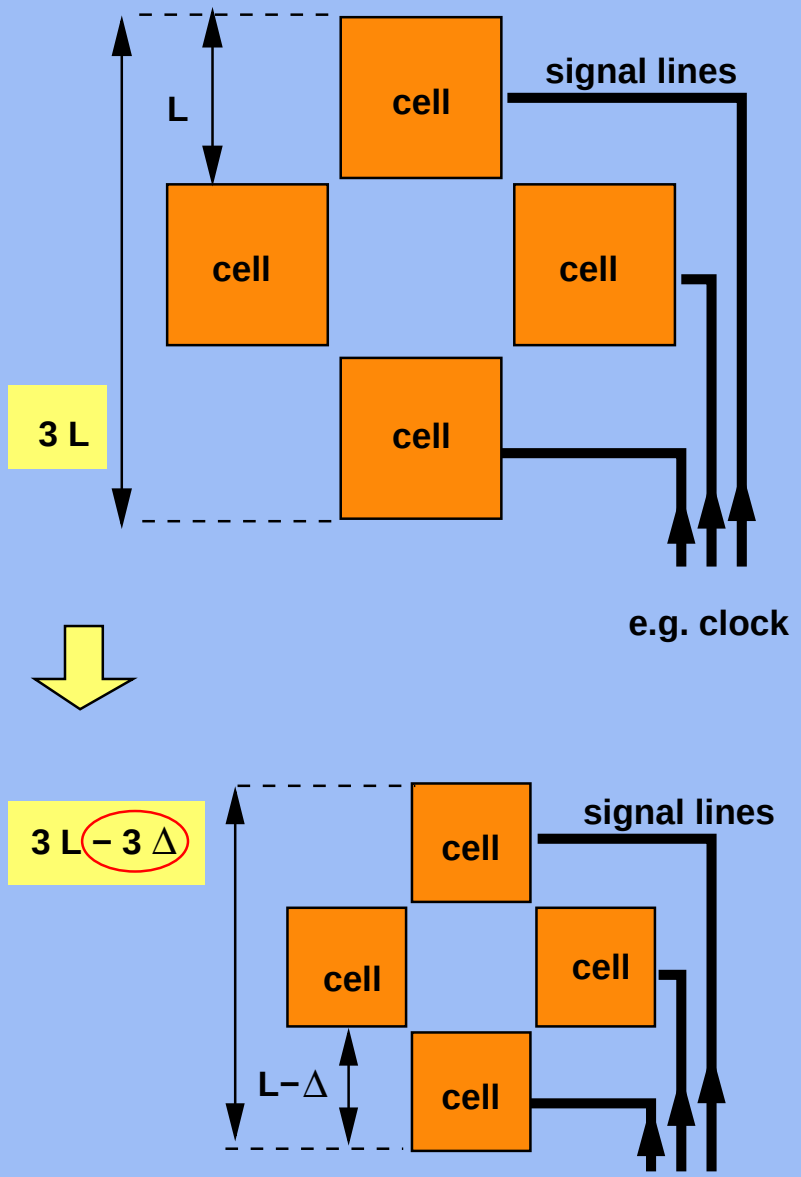
Optimization−Spiral

Device Size & Design Rules
(Max. Current densities ...
Min. Spacing/width, ...
Overlap, Doughnuts ...
Resistor type, sheet resistance...)

Driver power

Cell Size (L)

Transmission Line Lengths



High−Speed needs High−Support by Design Rules

Fig. 11

Bridgeover the Distance

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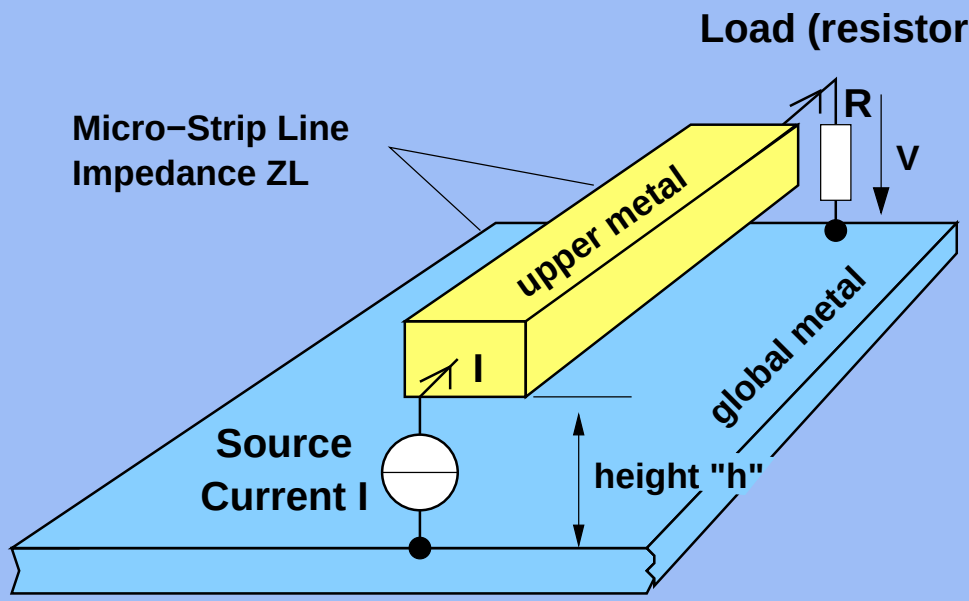
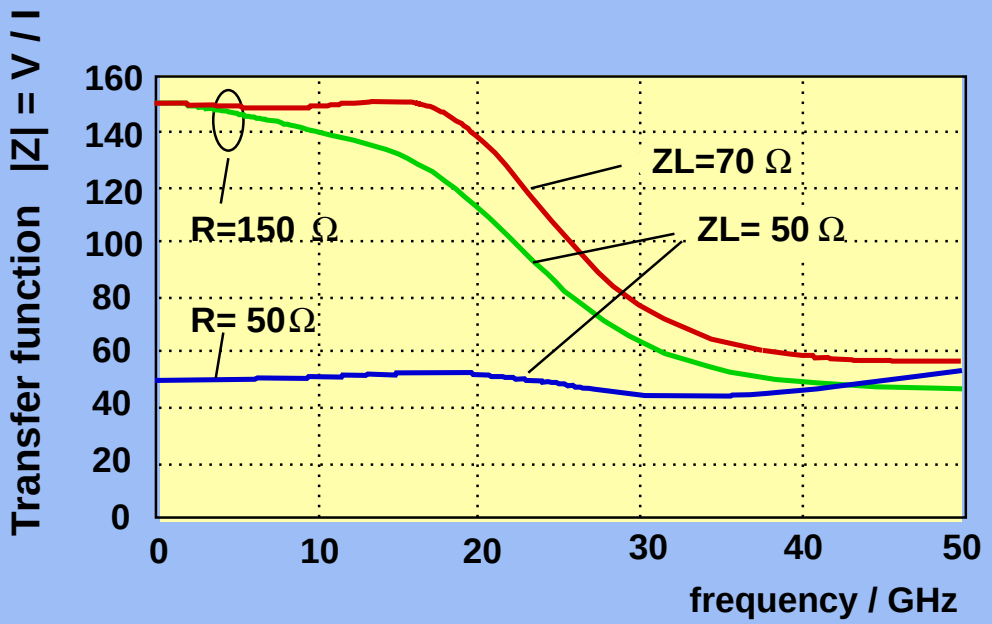
Constraint: Need for global metallization planes
(Power supply planes)

→ **Micro−Strip Lines**
(Supply plane is current return path)





Line Impedance ZL ~ $\sqrt{\frac{L}{C}}$

C ~ height "h"
C ~ epsr
L ~ 1/ line width ~ 1/C

Example in Fig.:
ZL=50 Ω → 70 Ω : h=2.2 μm → 4.4 μm

thick dielectric & low epsr → **high line impedance** → **high bandwidth (speed) & high gain (low power)**

Range of height and epsr limited: ZL < 80 Ohm

Fig. 12

Concept of Impedance Mismatch

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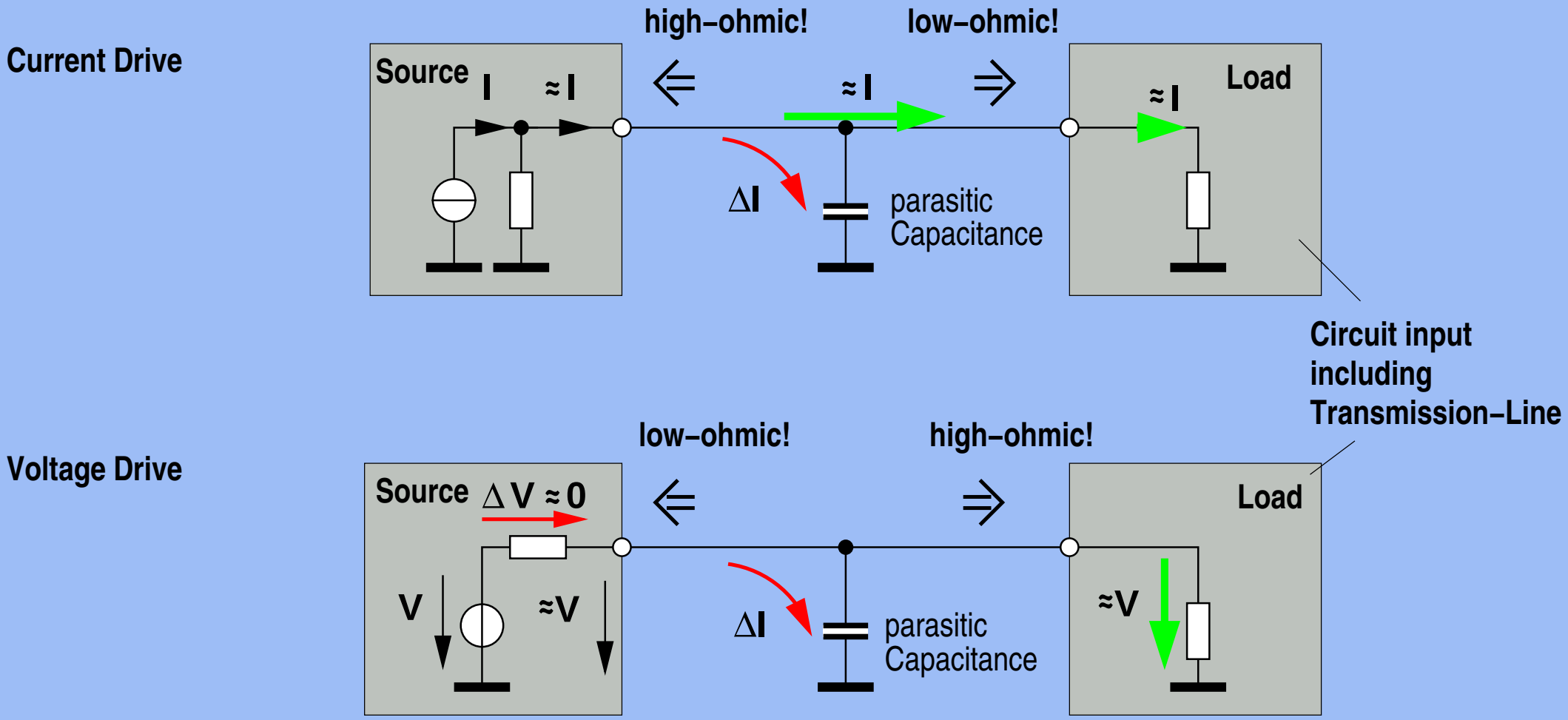

The More Mismatch ⇨ **The More Speed**

Fig. 13

High–Speed Circuit Topology

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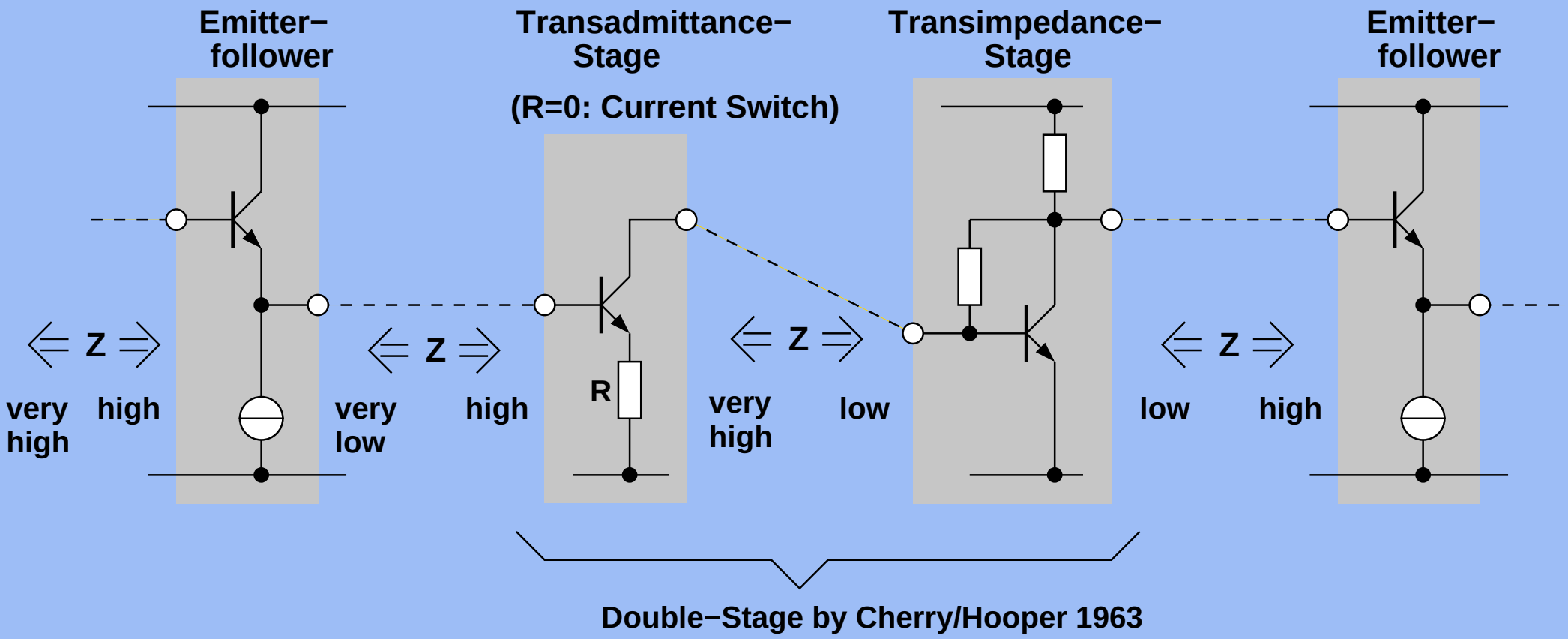
Example: Amplifier Stage



This is the Basic Principle Used in All High–Speed Circuits

Fig. 14

Complex–Conjugate Mismatch

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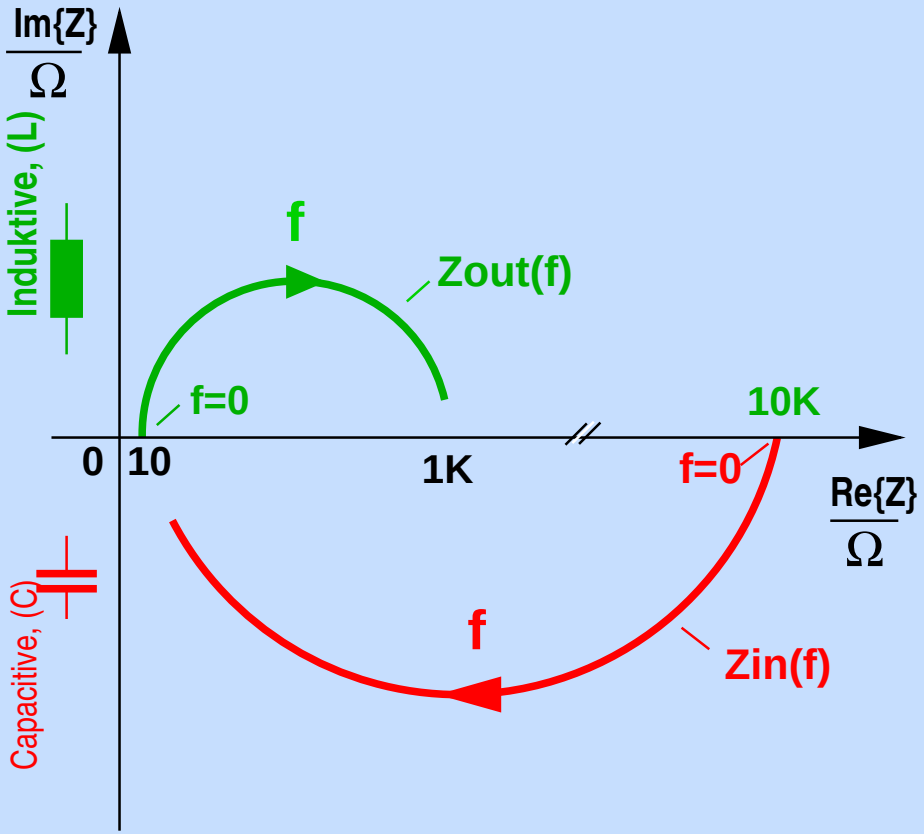
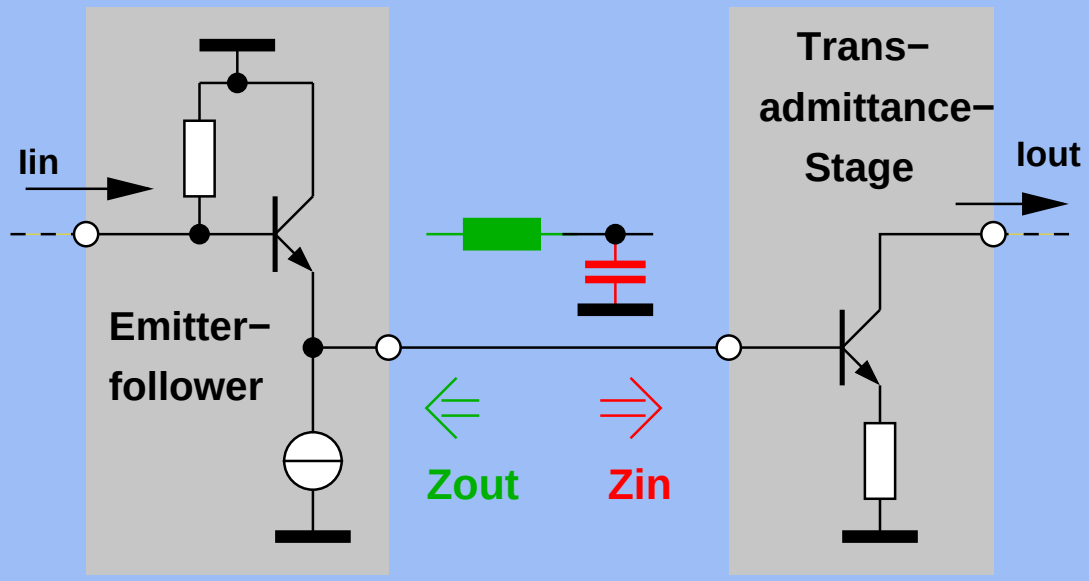
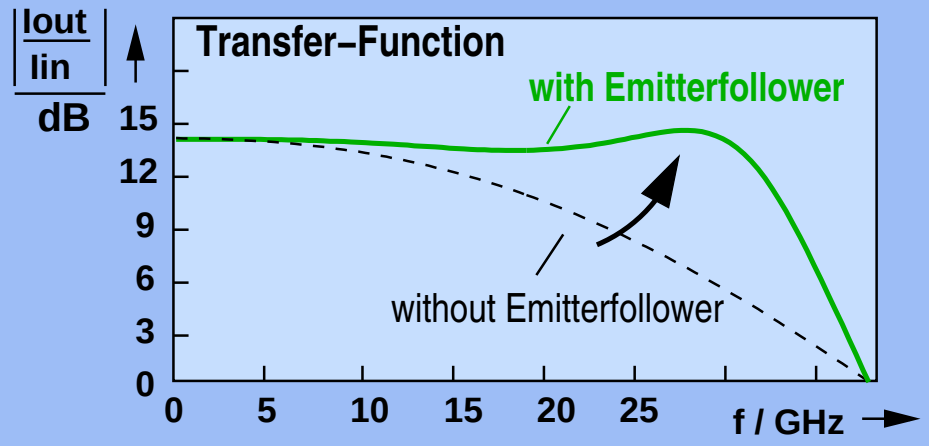
Impedance characteristics of Source & Load reverse as frequency increase







Utilize Complex–Conjugate Mismatch to Increase Speed

Fig. 15

Transistor = Impedance–Transformator

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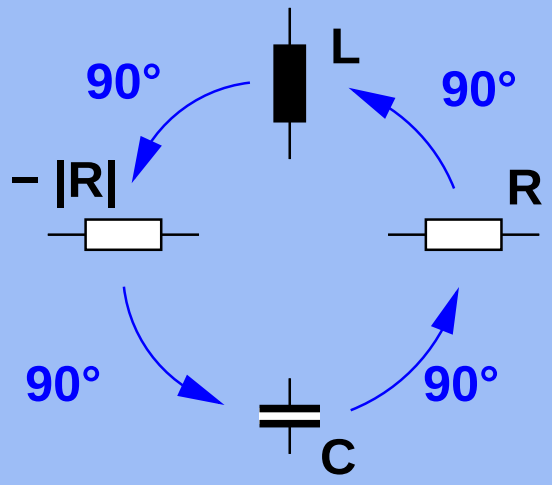
T–Operator:

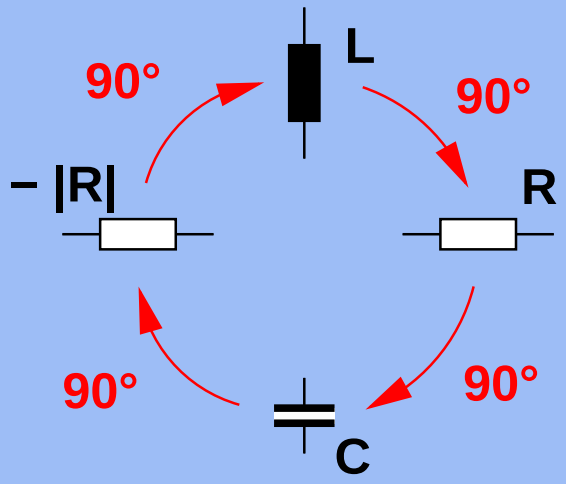
$$T \approx \frac{f_t}{j \cdot f}$$

Multiplication by T rotates Z by − 90° (clockwise)

Impedances at the Base appear rotated by 90° at the Emitter:



Impedances at the Emitter appear rotated by –90° at the Base:



Transformation Used to Optimize Pole/Zero Distribution of a Circuit

Fig. 16

Emitter–Follower Chain: A Tunable Resonance Network

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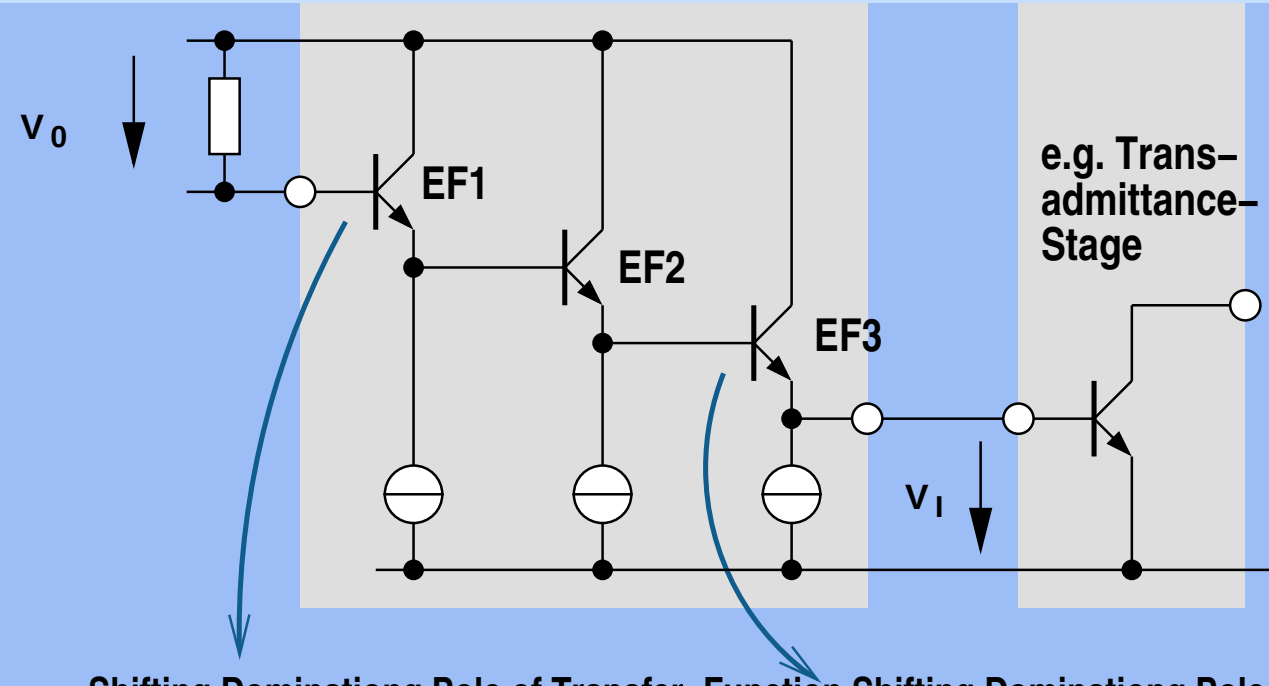
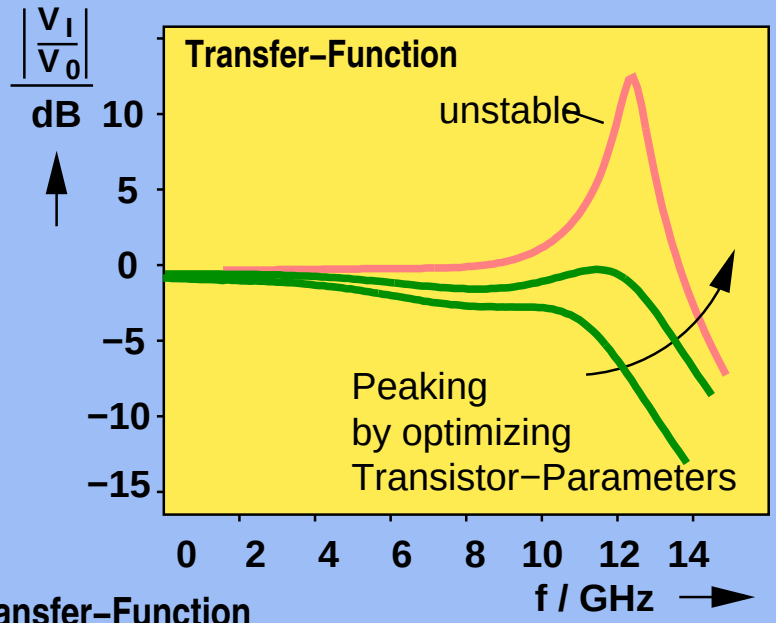
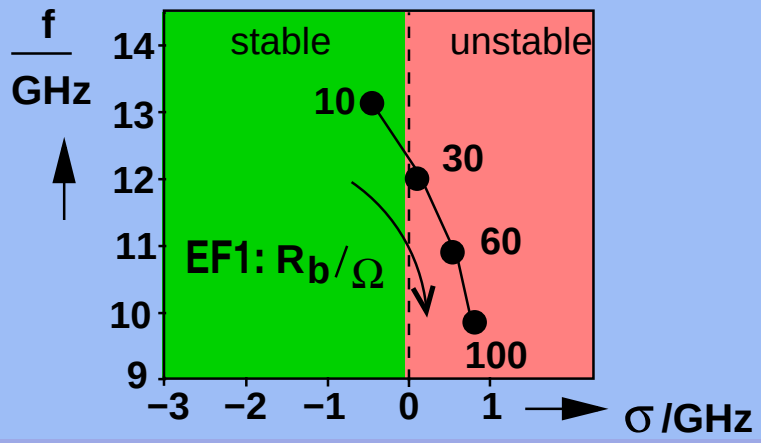
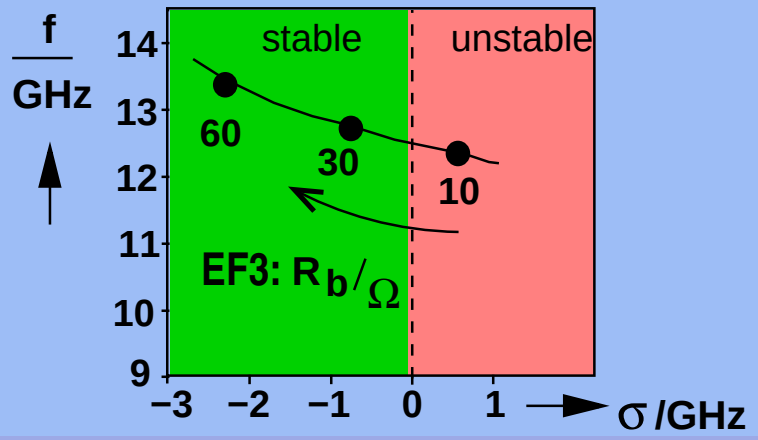




Shifting Dominationg Pole of Transfer–Function by Variation of EF1 Base Resistance



Shifting Dominationg Pole of Transfer–Function by Variation of EF3 Base Resistance



Great Opportunity to Increase Circuit Speed .... but ...

Fig. 17

Speed Optimized Circuits are Marginal Stable

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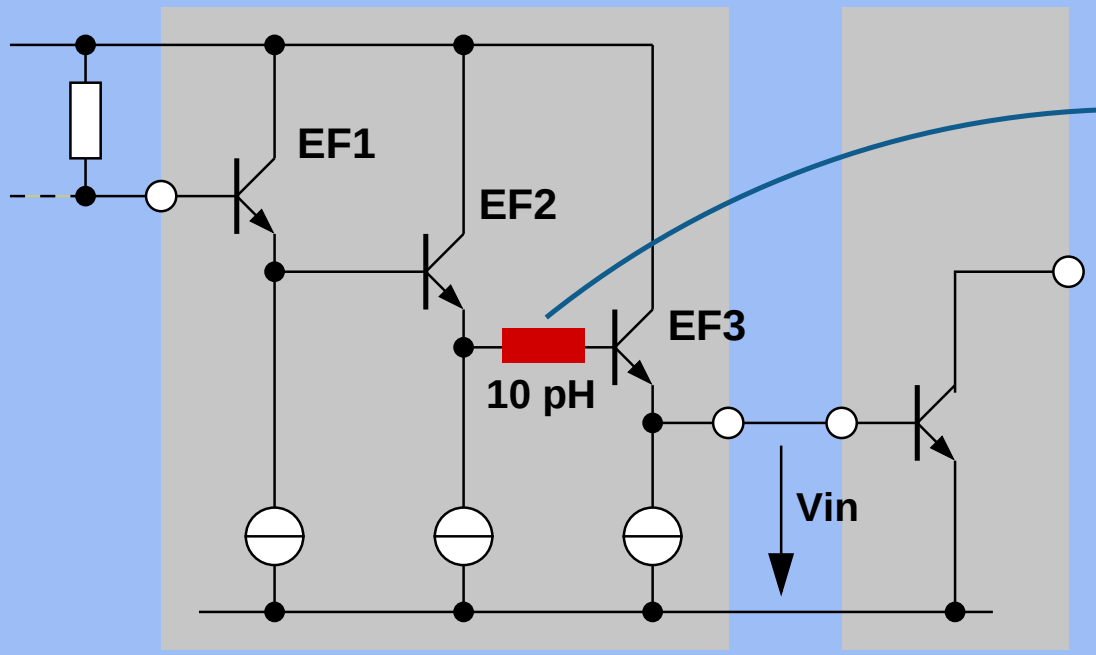
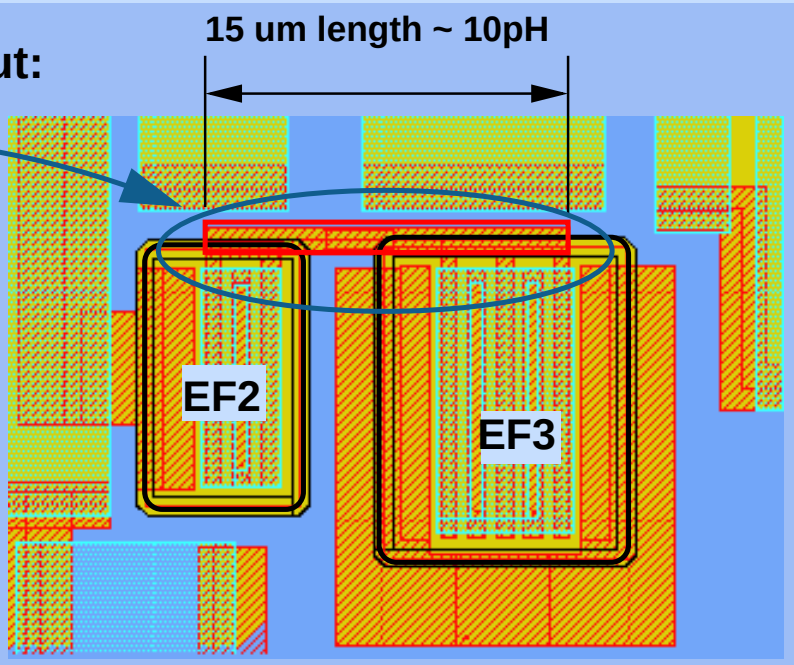
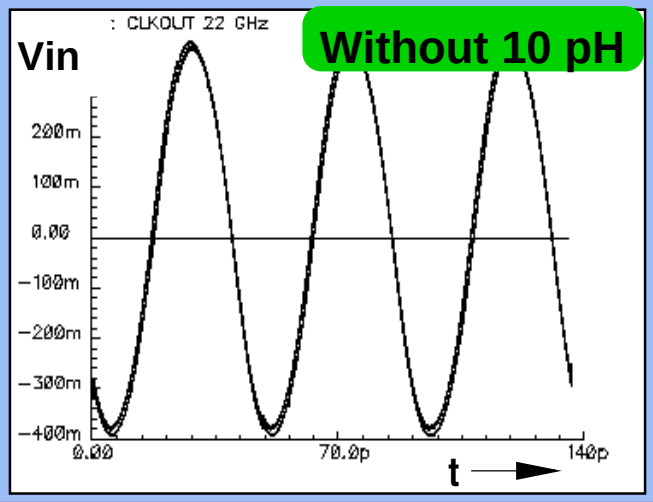
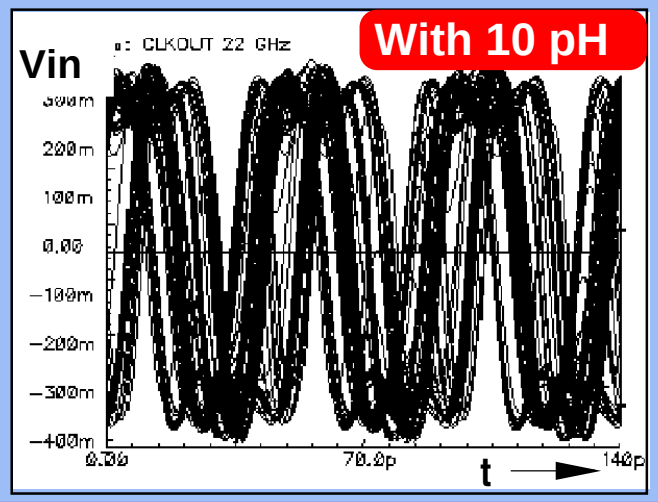


Layout:







Proof of Stability: Every Litte Piece of Metal is Suspicious!
Feedback Path might be different than Signal Path

Fig. 18

Fast Technology: Low Breakdown Voltage (V_{CE0})

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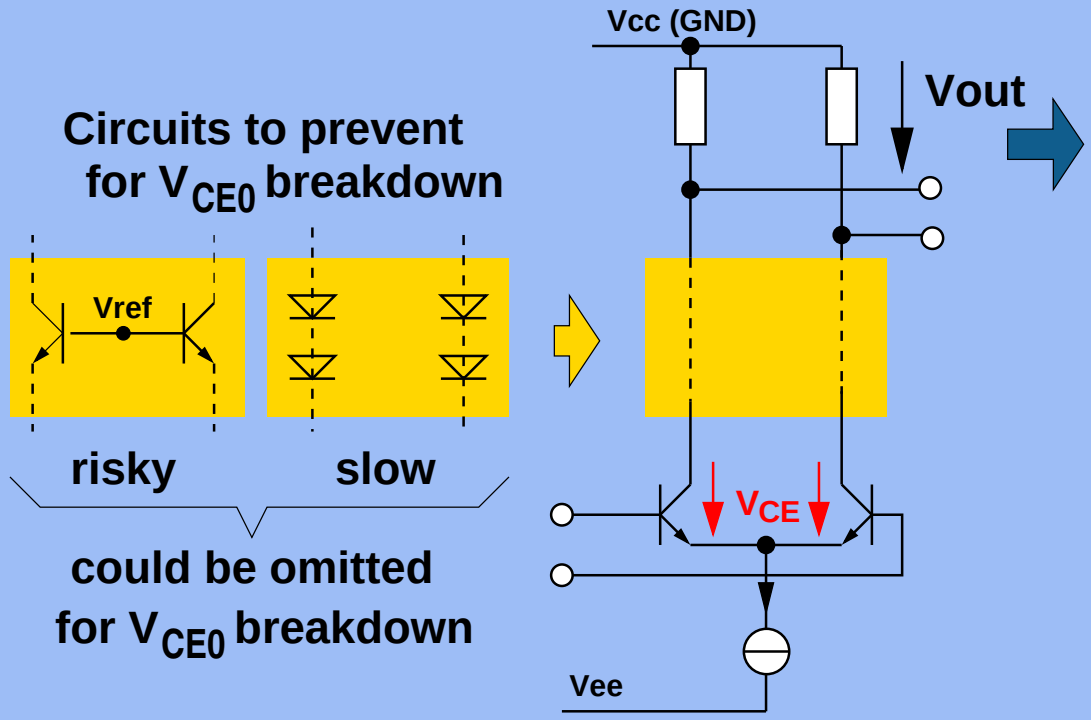

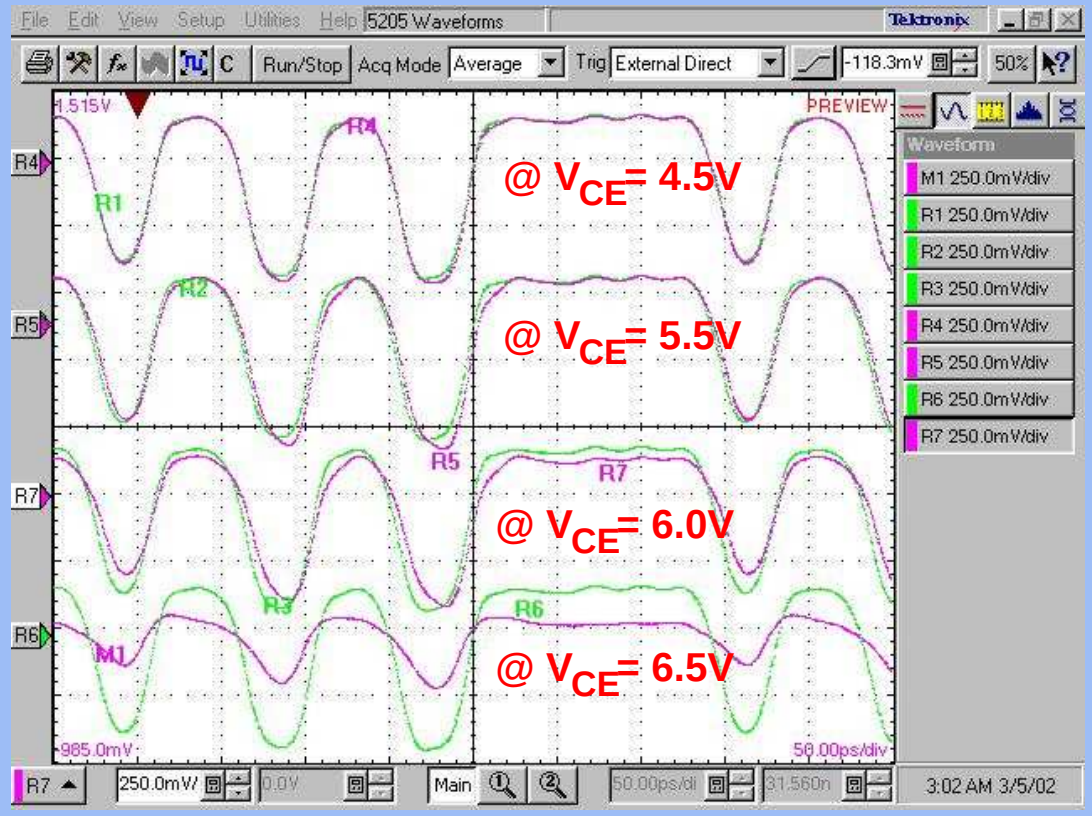

Example:
Limit given by technology V_{CEO} = 2.5V

Green trace: Reference Output–Voltage @ V_{CEO} = 2.5V

V_{CEO} Limit can be extended up to V_{CBO} by use of adequate Transistor–Models and Circuit Concepts

Fig. 19

Chip Assembly: High–Frequency Meets Precision Mechanics and Heat–Control

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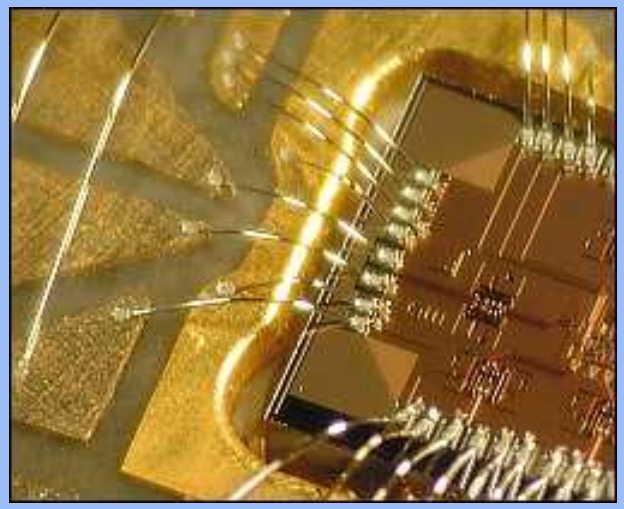

Design Goals: Small Inductances, High Thermal Conductivity

Fig. 20

Using Bondwires to Optimize the Strip–Line to Chip Interface

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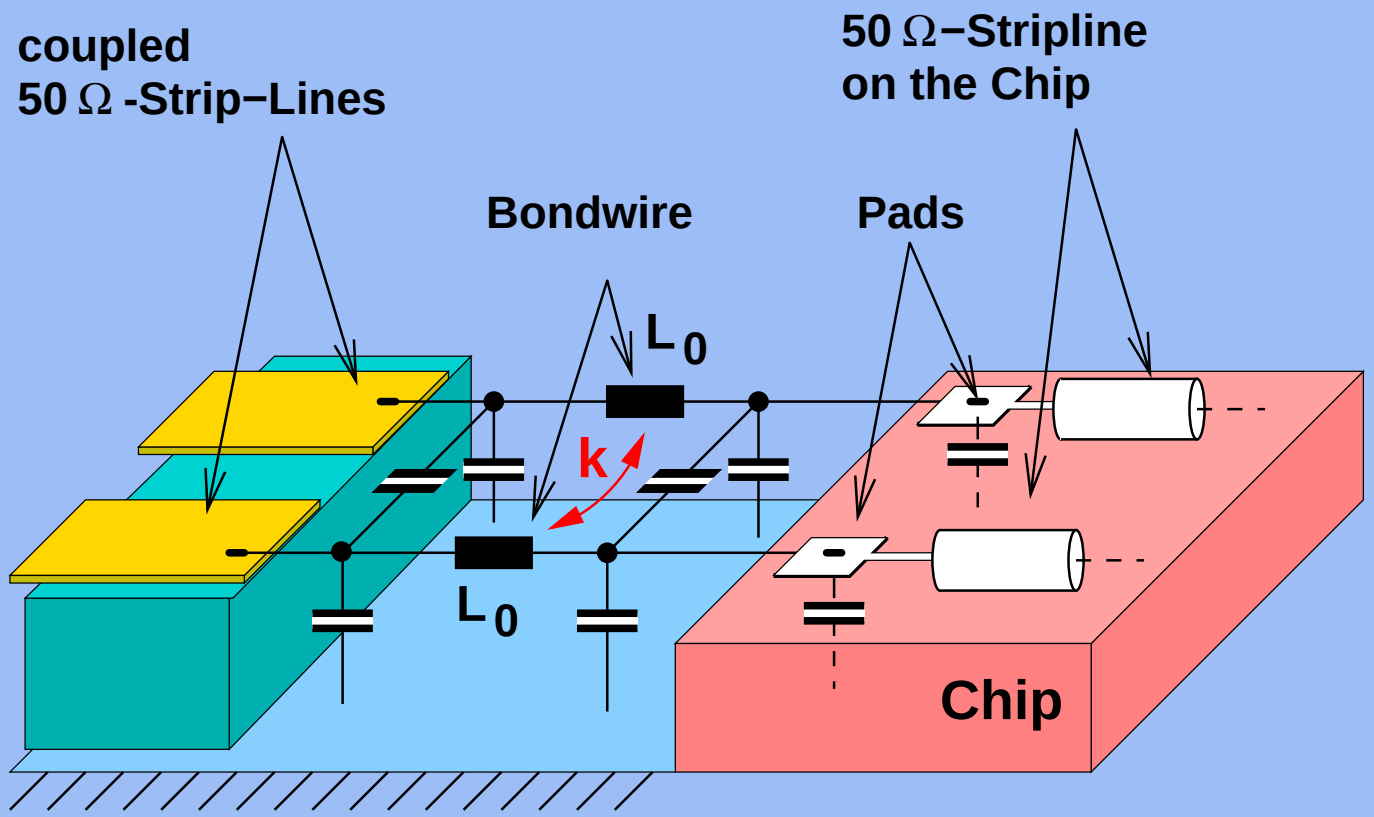
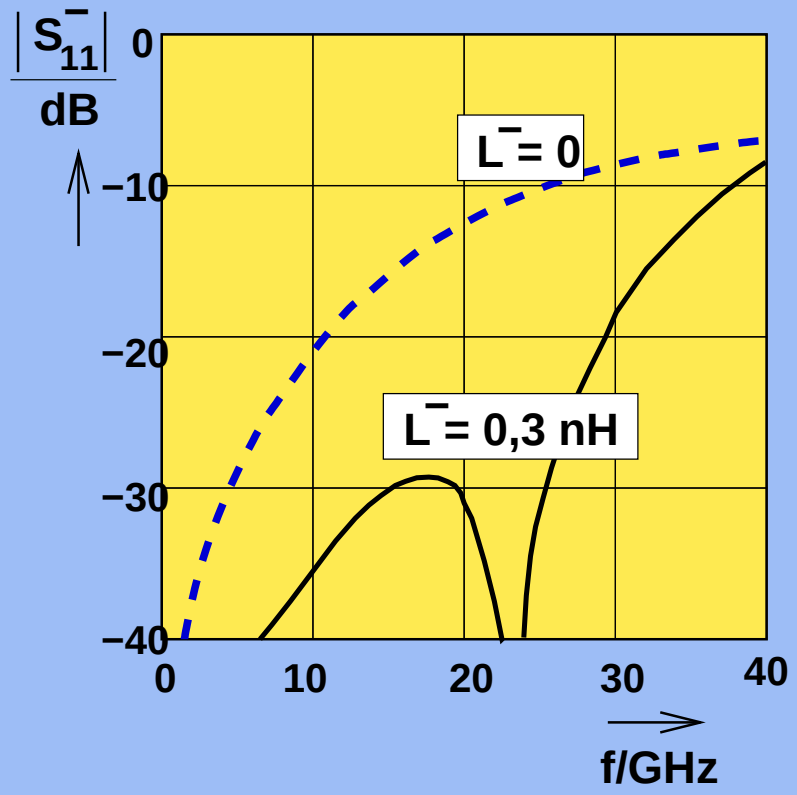
E.g.: Optimization of Refection Coefficient



Optimization goal:

$$Z_0^- \approx \sqrt{\frac{L^-}{\sum C^-}} \approx 50\ \Omega$$



$L^- = (1-k)\,L_0$ Odd–Mode–Inductance L^- can be adjusted by bondwire spacing

Bondwire can be used also for Noise– and Pulsshape–Optimization

High Speed = High Power Consumption

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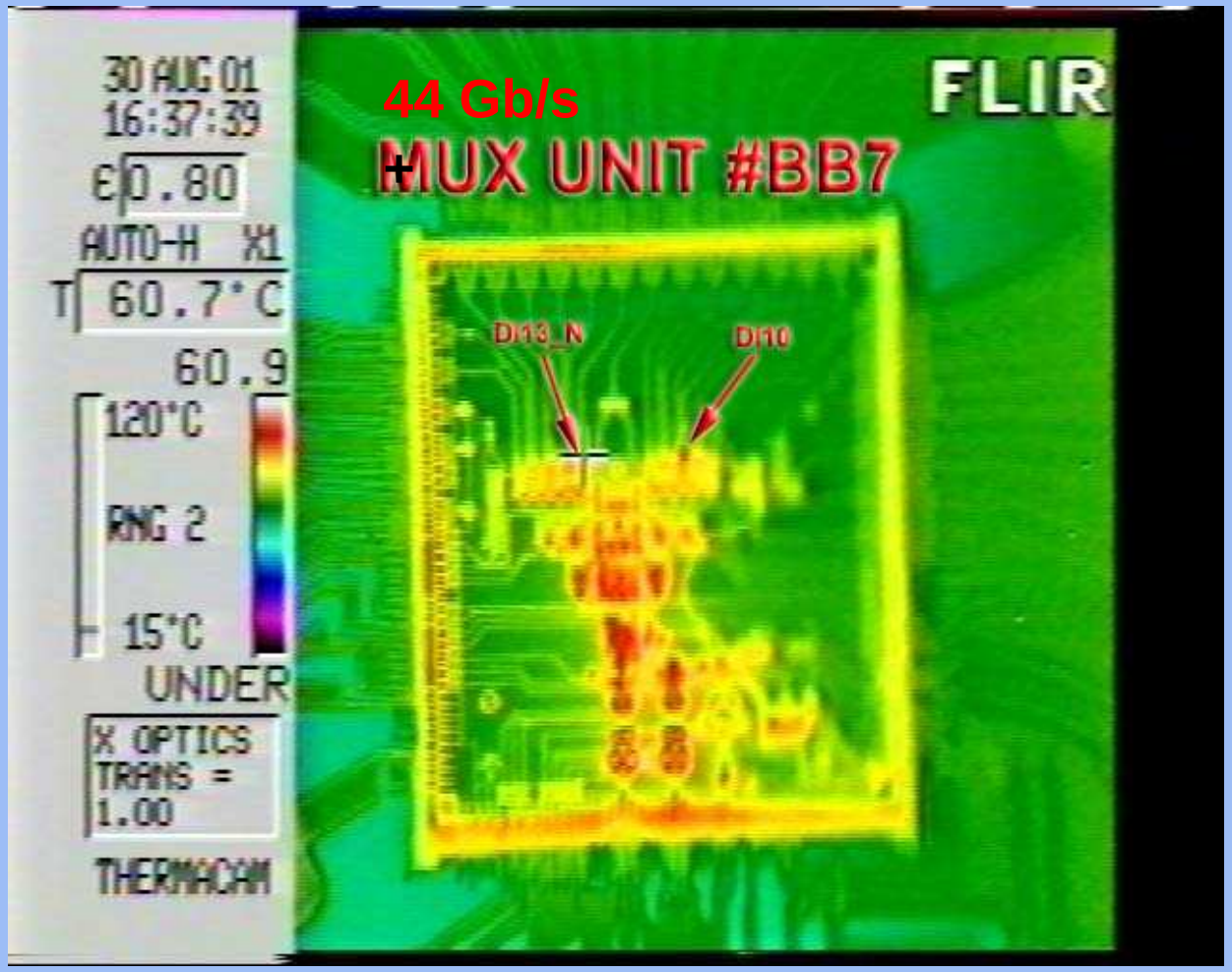

Power Density:

Chip: Your kitchen hot−plate:

$$1\ \frac{W}{mm^2} \Leftrightarrow 0.01\ \frac{W}{mm^2}$$

"Hot−Spots":

Areas of high power density lead to local heat concentration

"Self−heating"

Transistor heat up due to its own power

Time−constants in the ns−range!

Transistor cut−off frequency drops with increasing temperature:

Omit Hot−Spots → Spread Elements / Distribute Power Over Chip Area → But: Longer Wiring!

Fig. 23

Measurement of High–Speed Circuits

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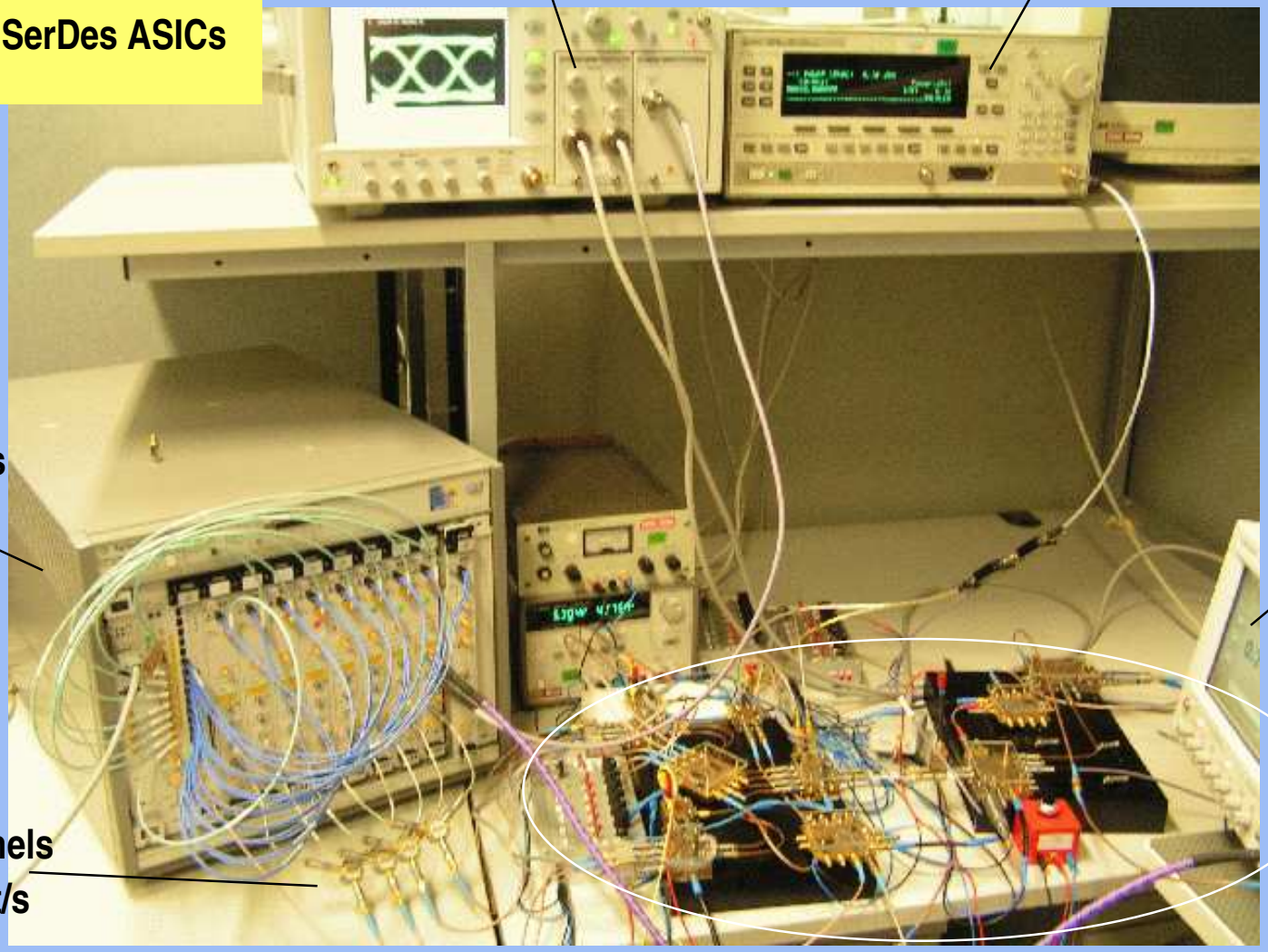
Actual Example:
Measurement of 100 Gbit/s SerDes ASICs



The Chicken and the Egg Dilemma

Fig. 24

Measurement of 100 Gbit/s MUX and CDR&DEMUX Modules

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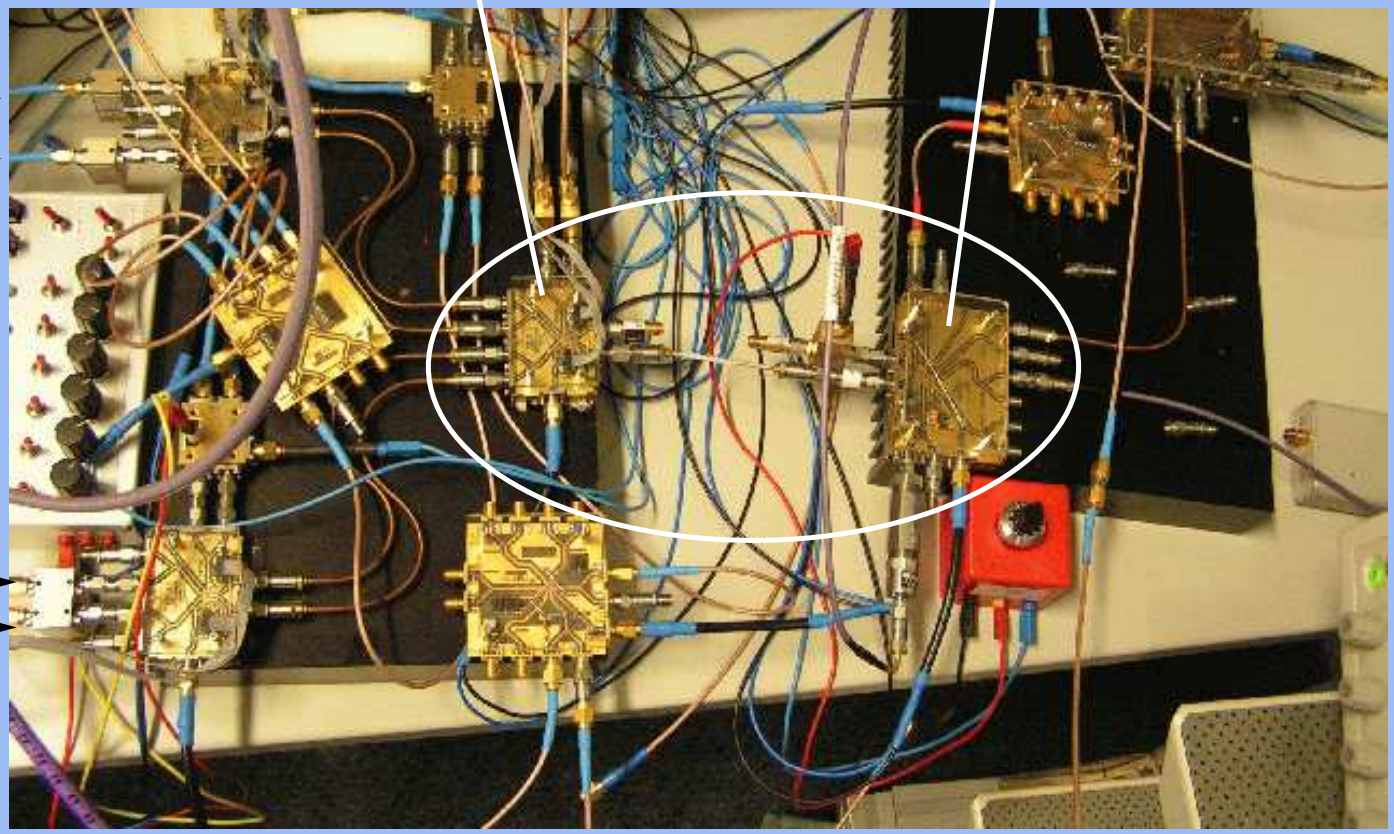
100 Gbit/s 2:1 MUX with automatic Clock–to–Data Timing Alignment

100 Gbit/s TIA & DEMUX (& CDR)



Input
4 x 25 Gbit/s

Output
1x12.5 Gbit/s

Measurement Concept with Auxiliary Circuits Must be Considered During Circuit Design

Fig. 25

100 Gbit/s Output Eye Diagram of 2:1 MUX Module

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- **Technologie:**
  Infineon B10HF
  f_T = 225 GHz
  f_{max} = 300 GHz
- **Outputsignal:**
  320 mVpp, single ended
  < 400 fs Jitter

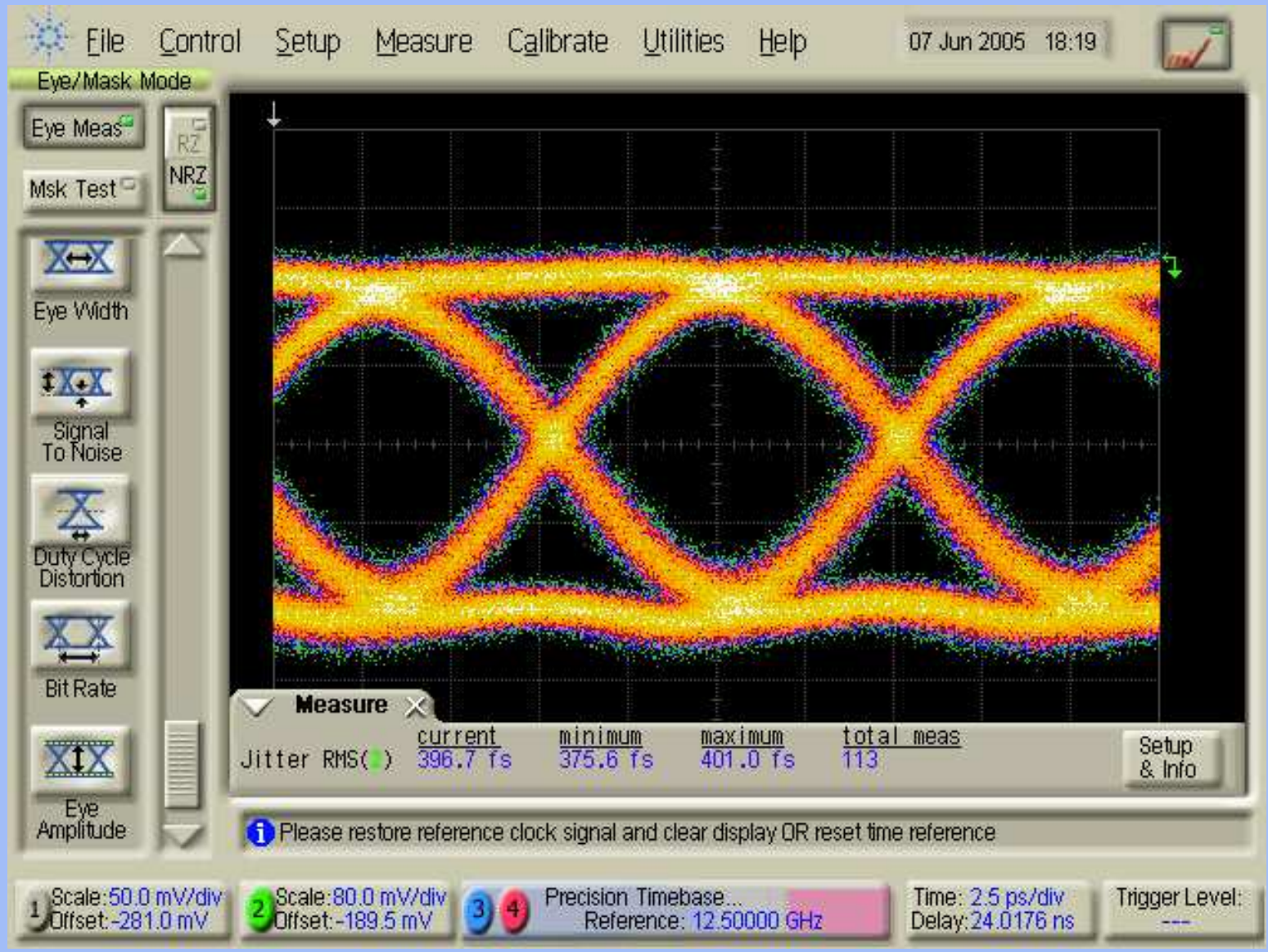

Fig. 26

86 Gbit/s Reveiver (TIA, DEMUX, CDR, VCO) with On–Chip PLL

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- German BMBF–Project:

  MultiTeraNet

- Technology:

  Infineon B10HF

Measurement Results:

- Min. Input Voltage (BER=0):

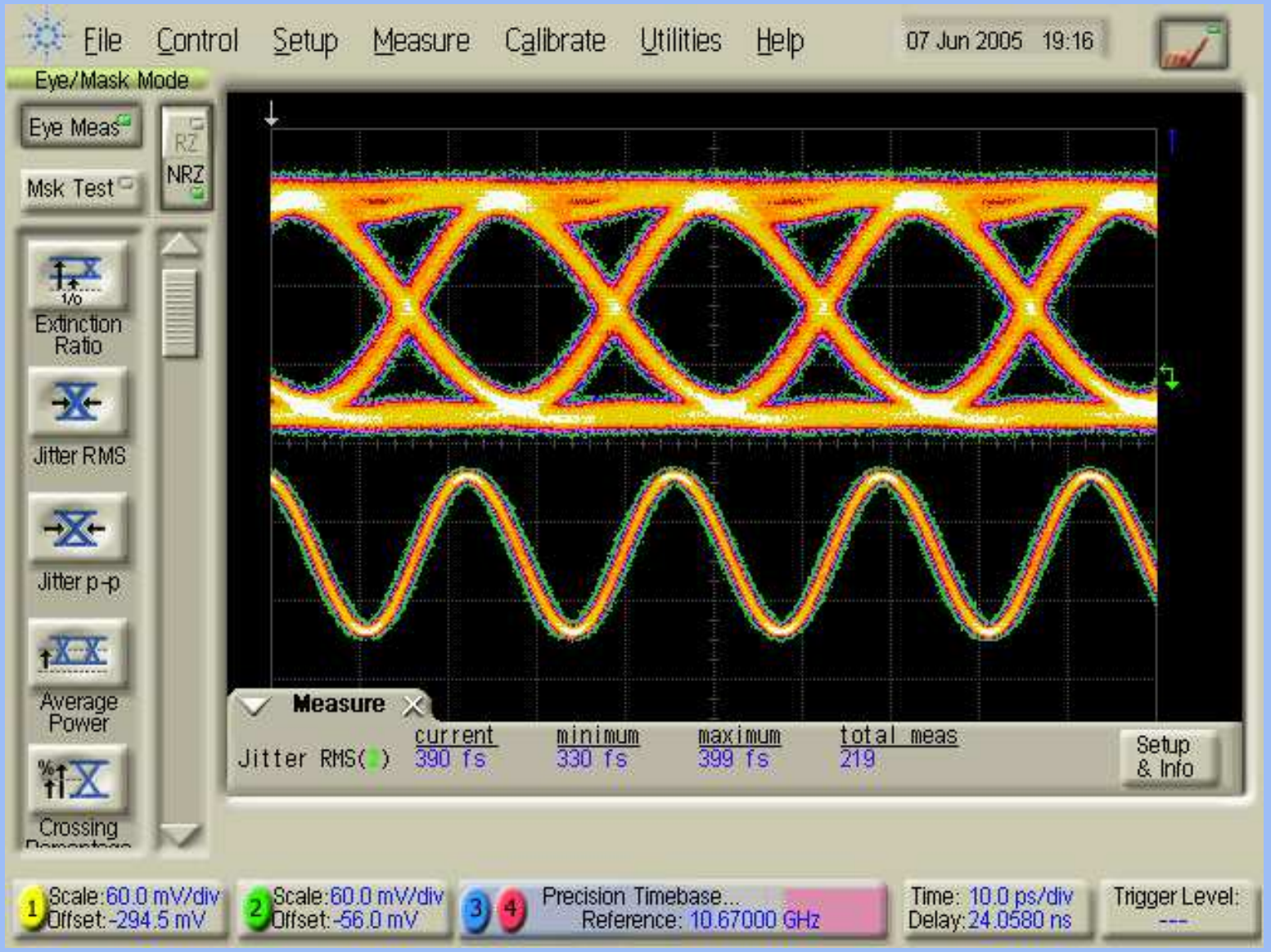
  < 30 mV single ended

- Recovered Clock:

  < 400 fs Jitter

- With Exteral VCO (50 GHz):

  100 Gbit/s (BER=0)



That's it for Today – Thank You!