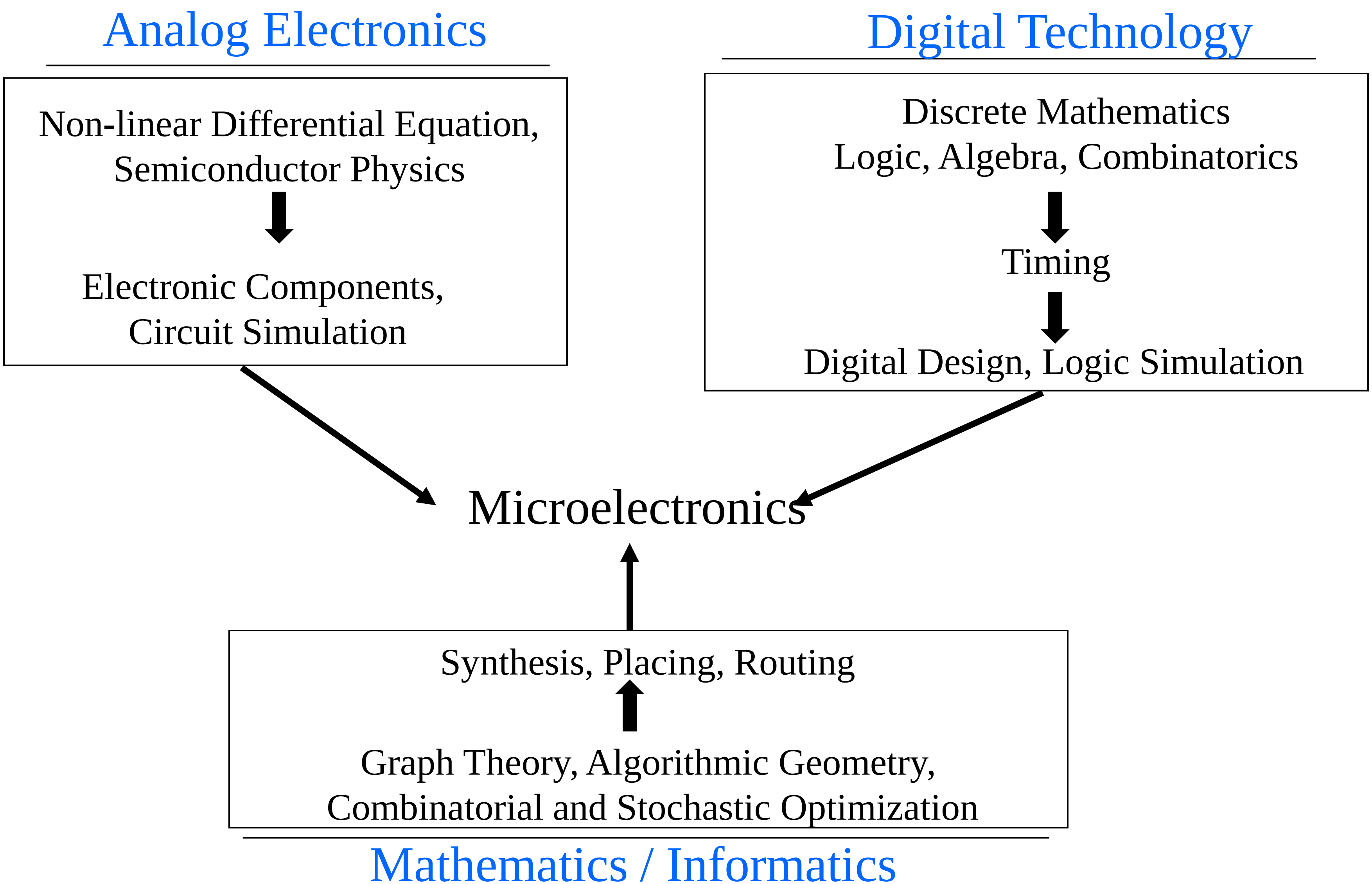
Technological Basics of Microelectronics



Levels and perspectives of Microelectronics

Semiconductor Level

Partial differential and physical equations

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Circuit Level

Models for components

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System Level

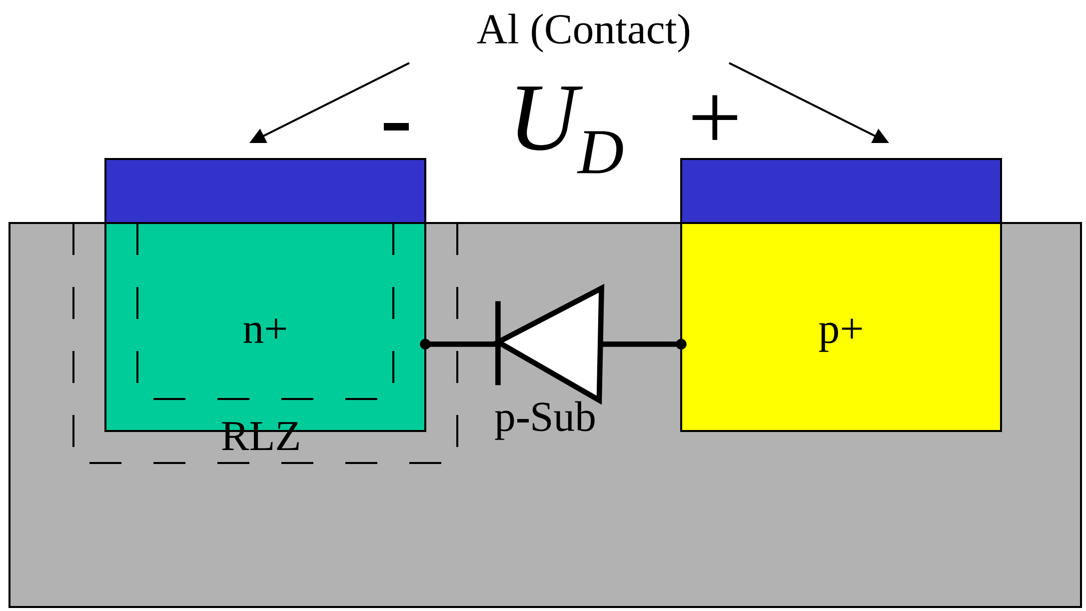
Functions for applications

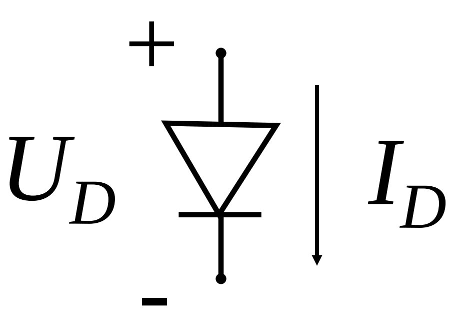
Standard Components of IC-Process

- Transistor
  - Bipolar
  - MOS
- Diode
- Condensator
- Resistor
- no Inductor and Transformer

A process may have several components of the same kind, but with different parameters.

Realization of a Diode

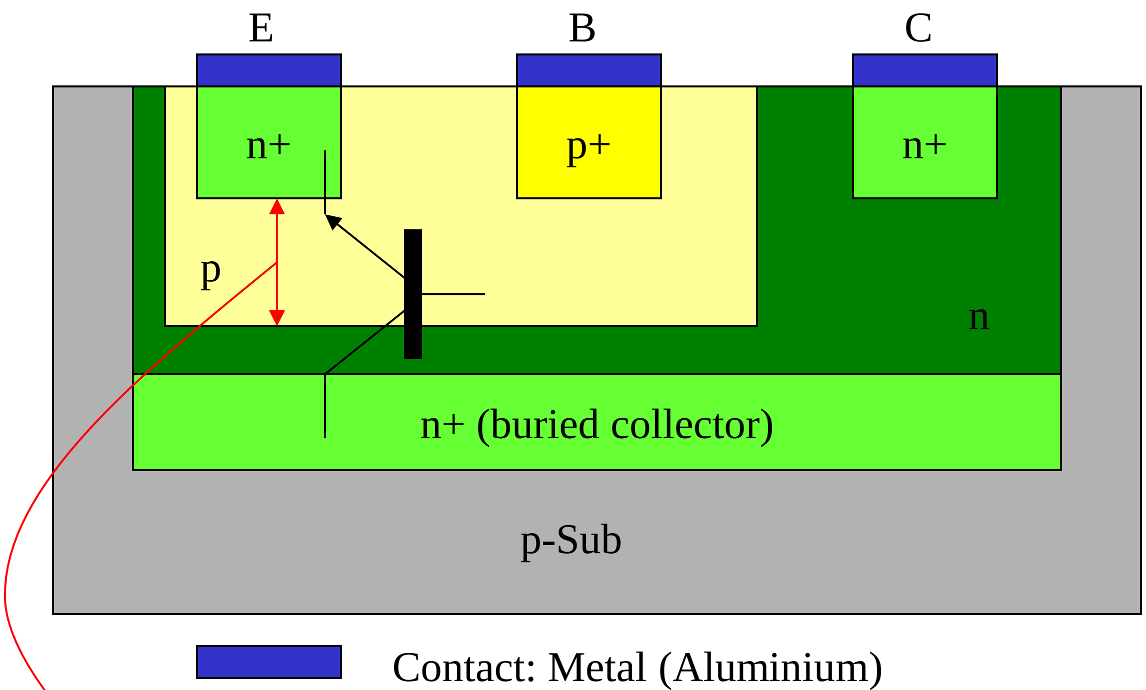


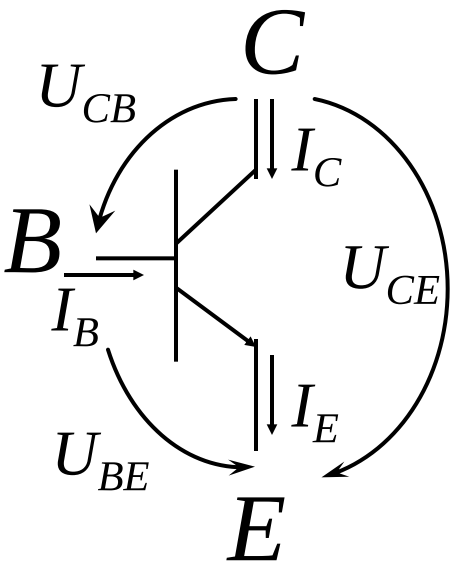


Currrent equation of Diode:

$$I_D = I_s\left(e^{\left(U_D / n \cdot U_{Temp}\right)} - 1\right)$$

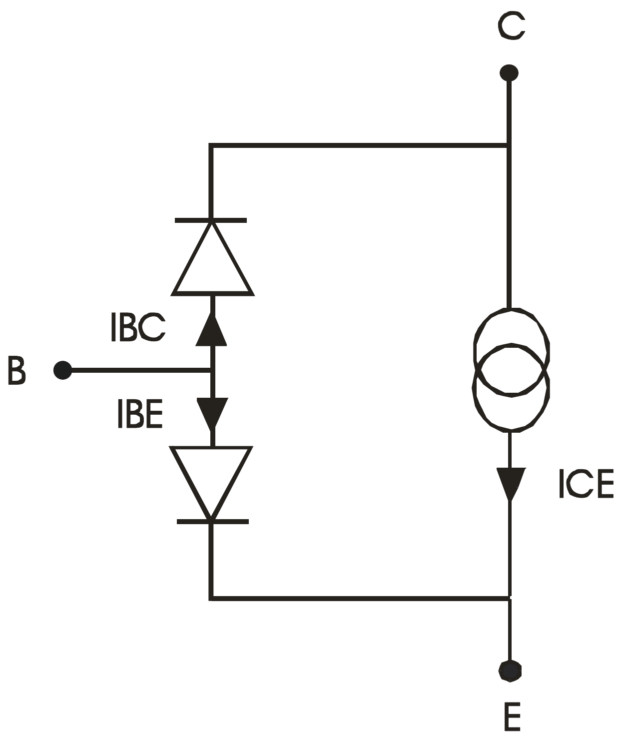
Realization of a Bipolar-Transistor





Where is the most important parameter ?
Base width

Gummel-Poon-Model for BJT



$$I_{BE} = \frac{I_s}{B_f}\left(e^{\frac{U_{BE}}{n_f U_T}} - 1\right)$$

$$I_{BC} = \frac{I_S}{B_r}\left(e^{\frac{U_{BC}}{n_r U_T}} - 1\right)$$

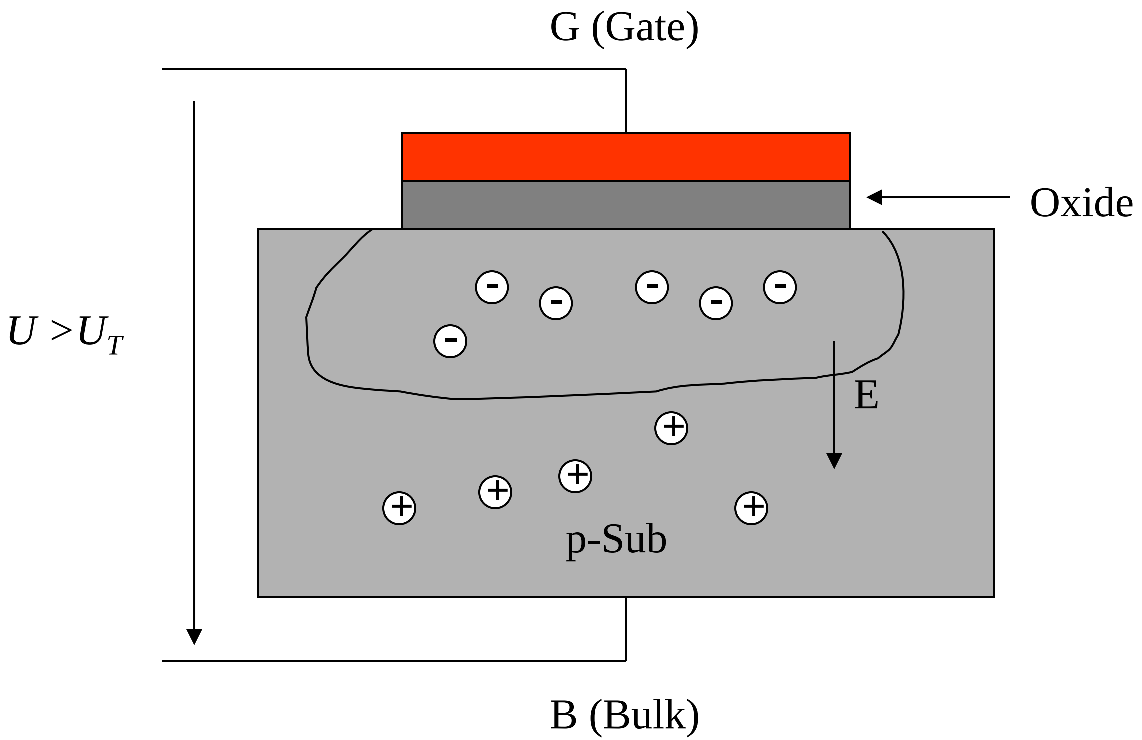
$$I_{CE} = \frac{I_s}{q_B}\left(e^{\frac{U_{BE}}{n_f U_T}} - e^{\frac{U_{BC}}{n_r U_T}}\right)$$

B_f: forward gain
B_r: reverse gain
q_b: standardized base charge under consideration of the Early-effect and high-current effect

Realization of a MOS-Condensor

(**M**etal **O**xide **S**emiconductor)

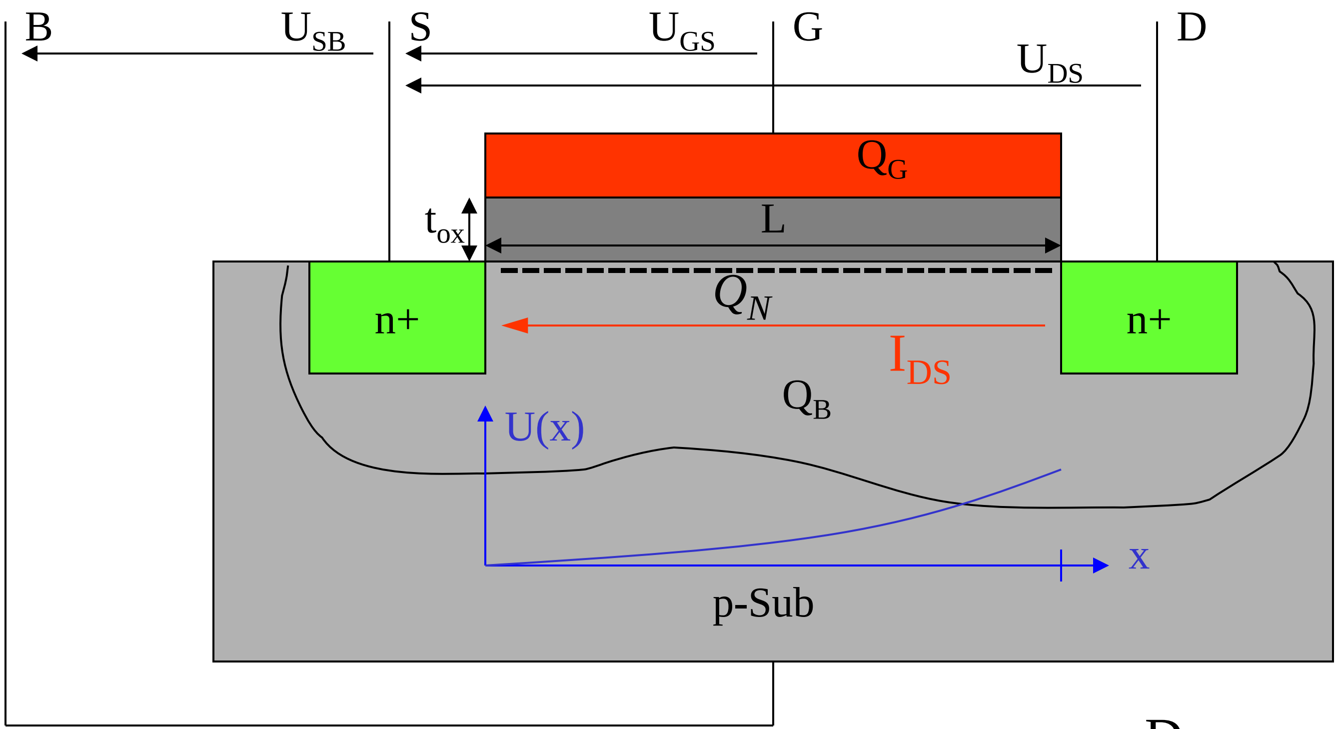
MOS-Condensor and its space charge zone



Vg positive: Inversion

Vg negative: Accumulation

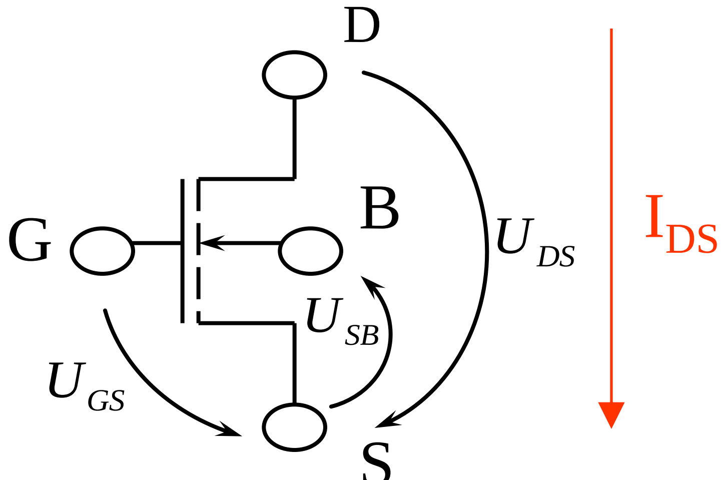
Realization of a MOS Transistor



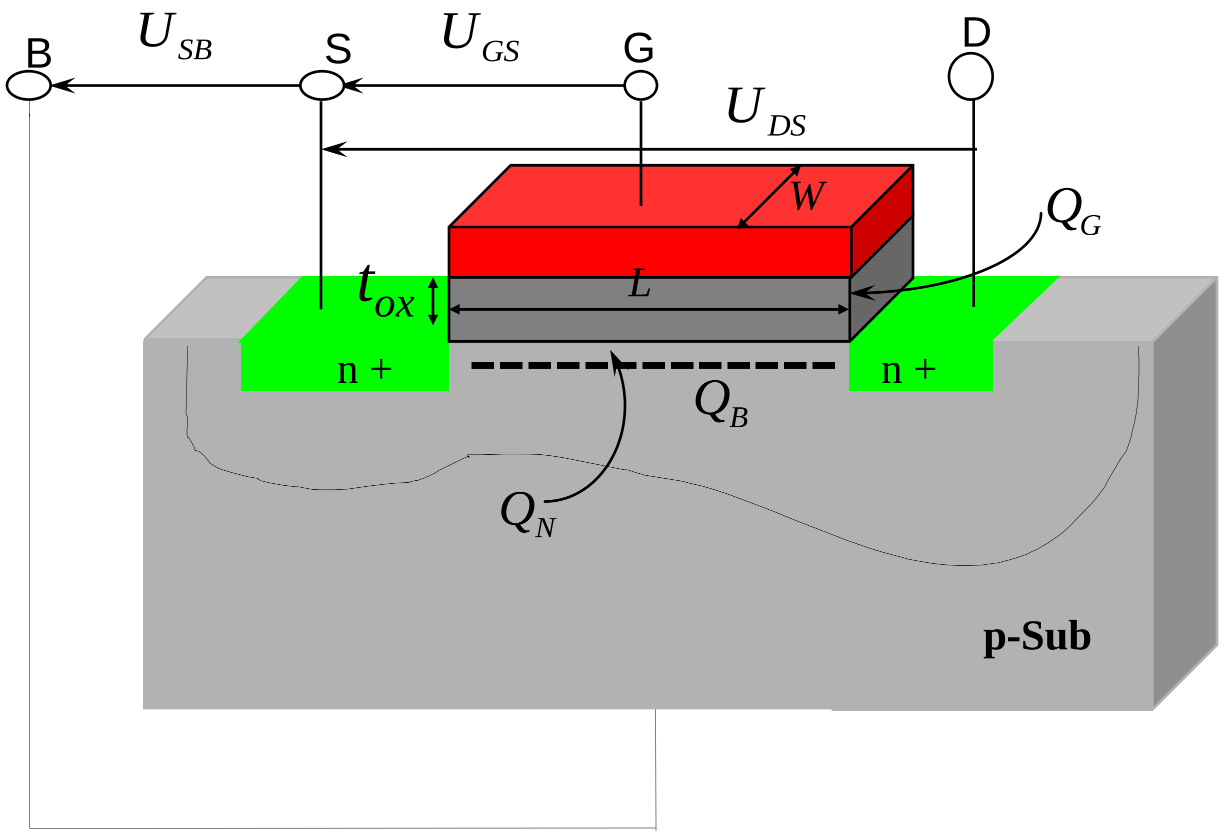
Q_G: Ladung auf dem Gate

Q_N: Ladung im leitenden Kanal

Q_B: Ladung in der Raumladungs zone unter dem Gate

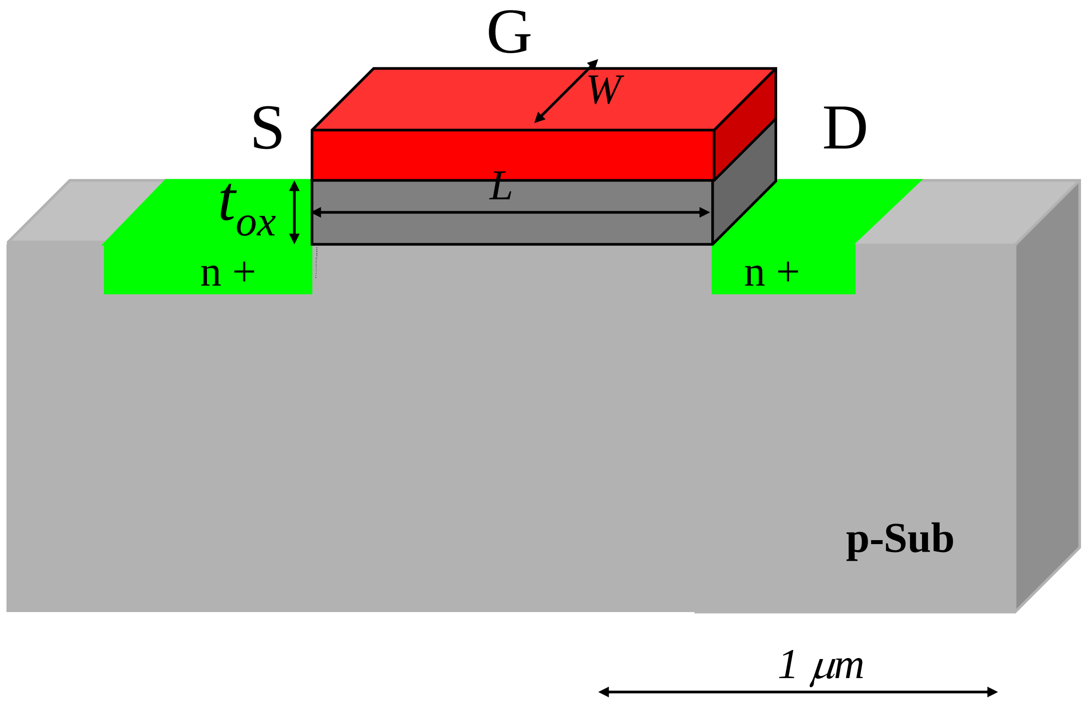


3-D View of a MOS Transistor



The transistor can be realized in a p-well instead of substrate.
Many transistors can be realized in one and the same well .

Structure dimensions



Examplary values: L = 1 µm

W = 0,5 µm

t_{ox} = 100 åm

W and L are circuit (design) parameters

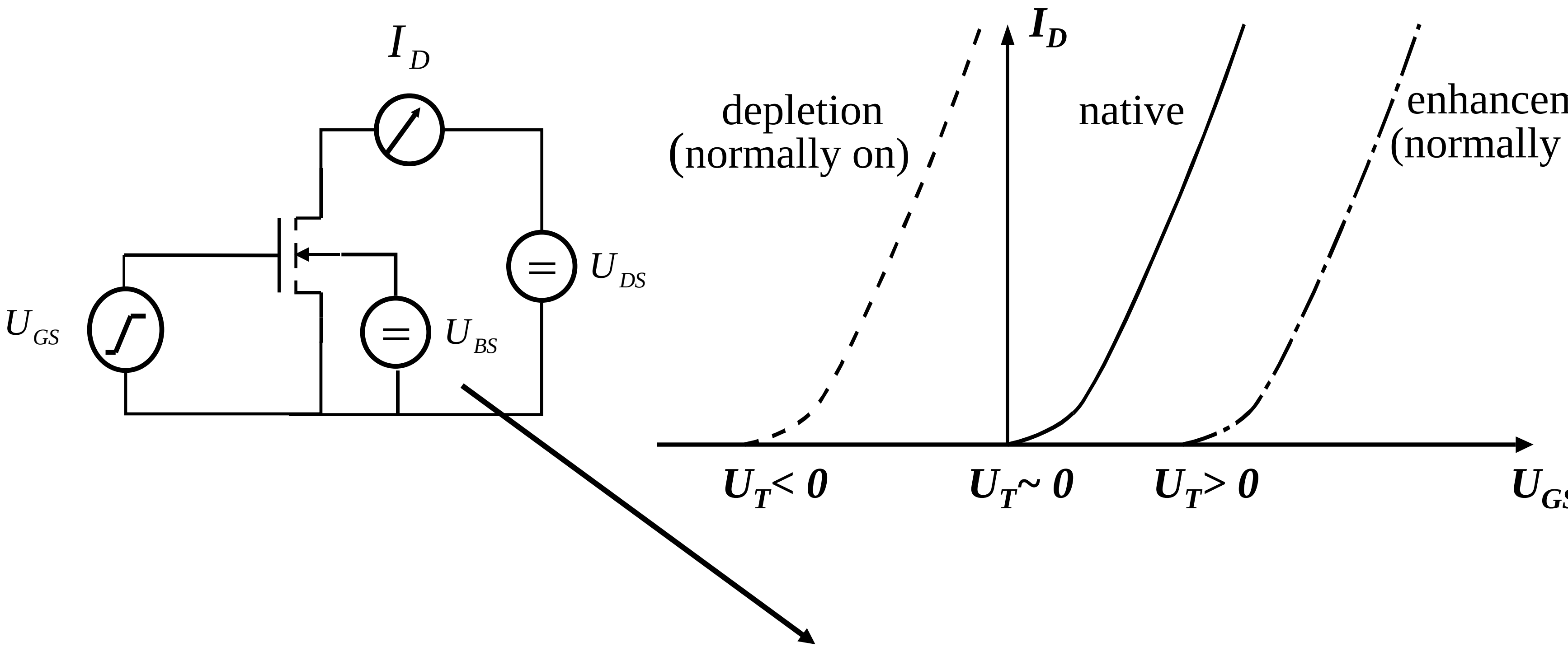
tox process parameters

Advantages of a MOS-Transistor

- High input-resistance (no input current)
- Gate-capacity can be used as storage element
- Symmetry (Drain and Source are electrically equivalent)
- Due to lateral structure easy to be shrinked
- Electrical characteristics improve with smaller structure

Transfer Characteristic

Vds = constant > 0, Id = f (Vgs)

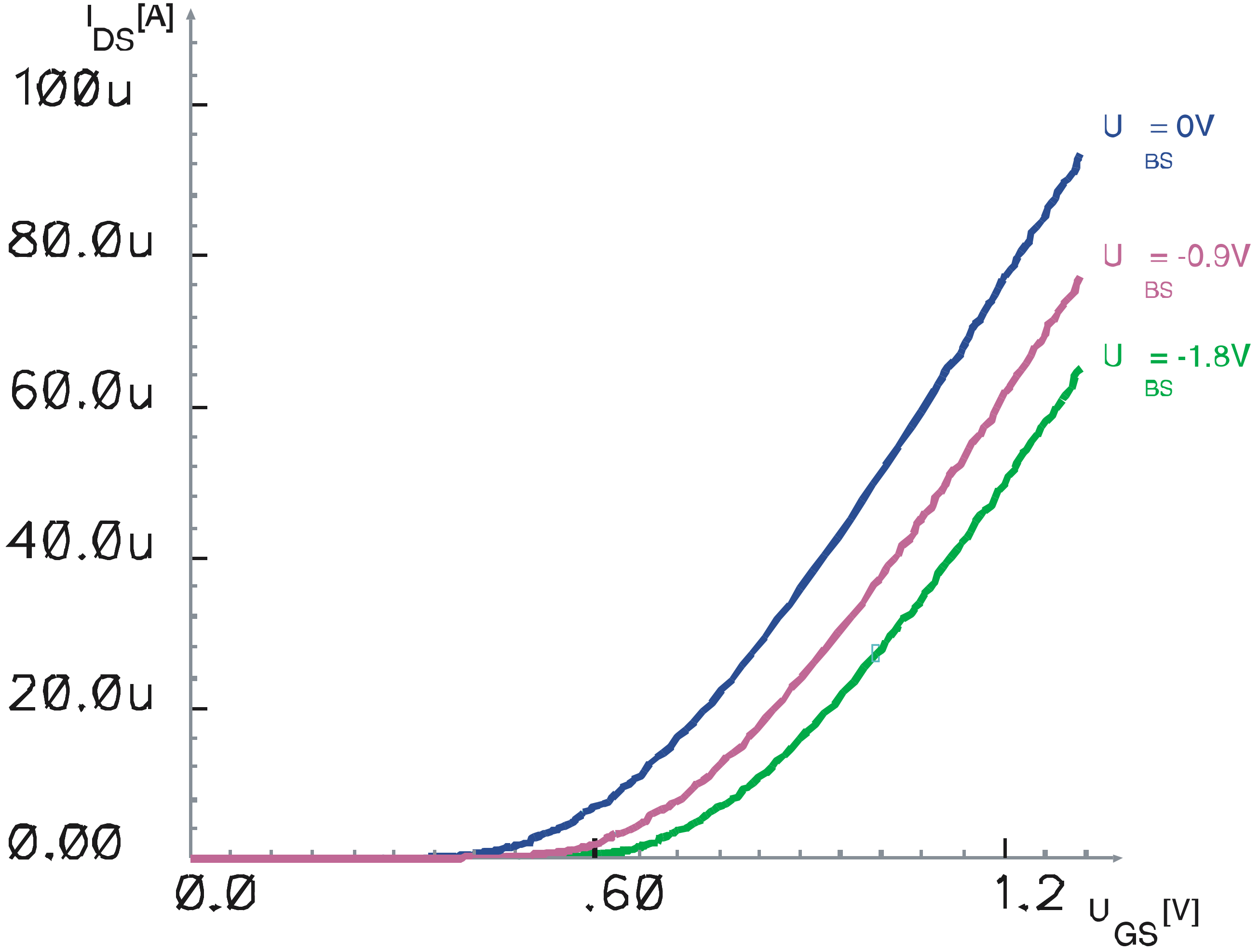


$$U_T = U_{T0} + \gamma \ \left(\sqrt{U_{SB} + 2 \cdot \varphi_D} - \sqrt{2 \cdot \varphi_D}\right)$$

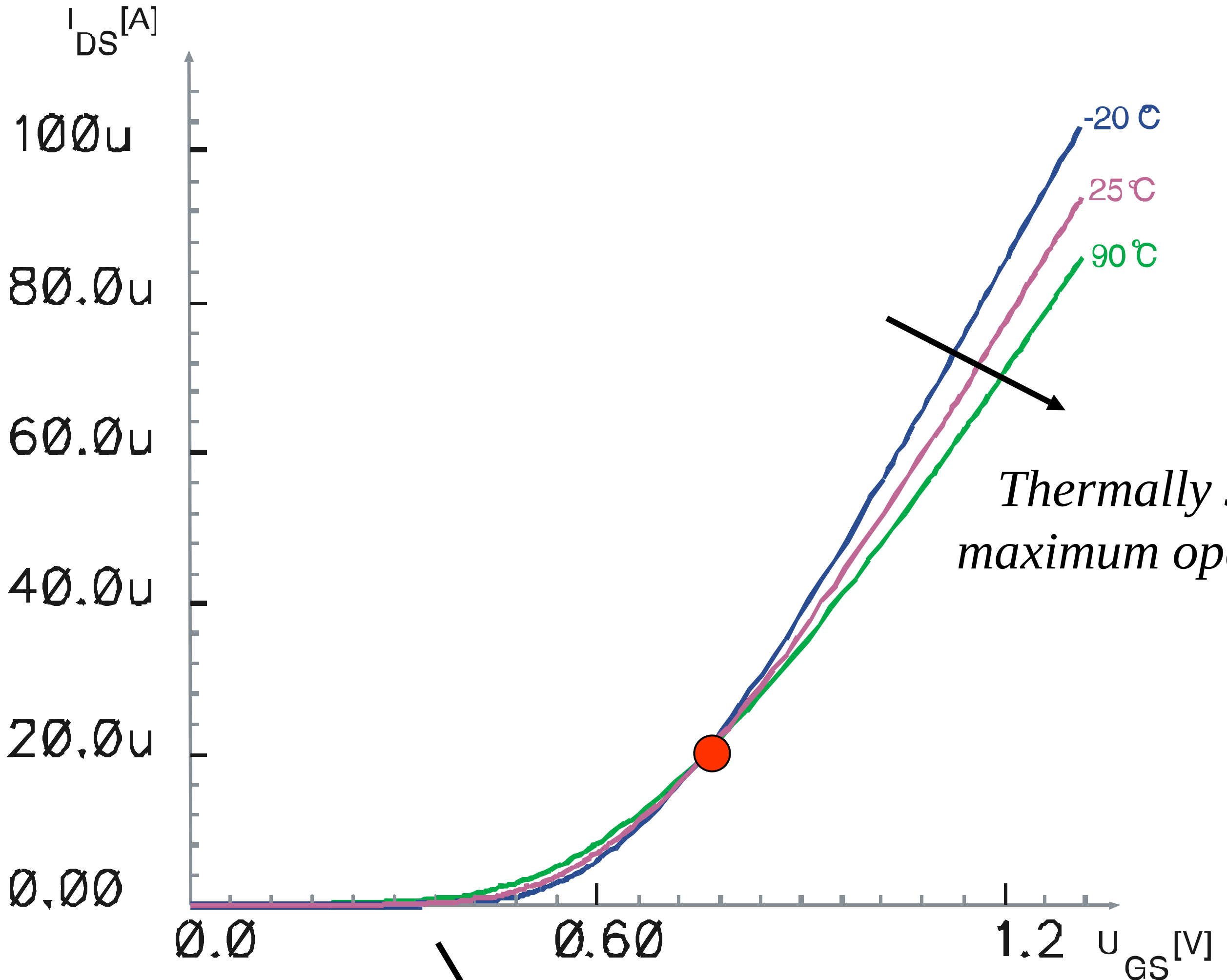
More gate charge necessary for compensating the bulk charge

Transfer characteristic in dependence of Usb

$$U_T = U_{T0} + \gamma \; \left(\sqrt{U_{SB} + 2\cdot\varphi_D} - \sqrt{2\cdot\varphi_D}\right)$$



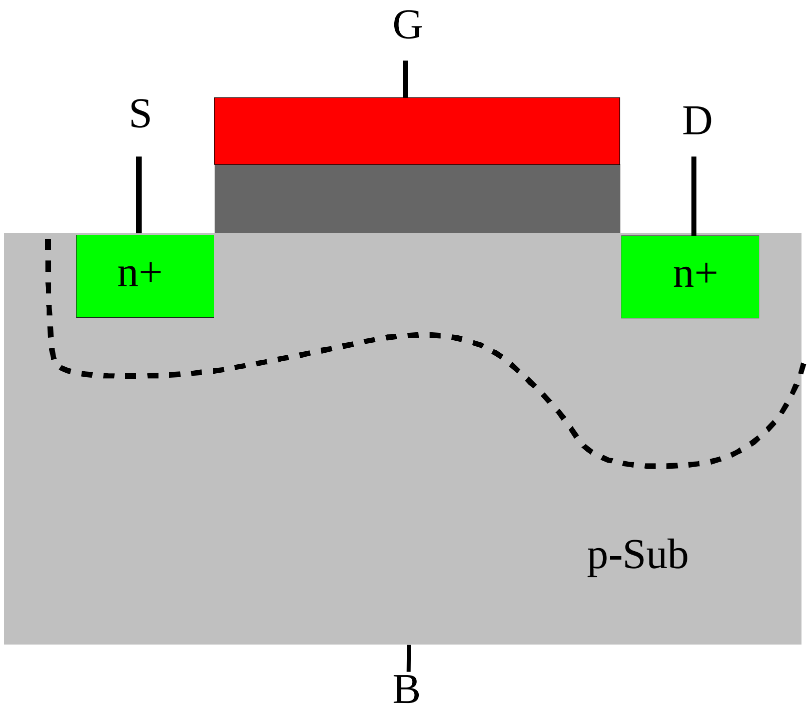
Transfer characteristic in dependence of temperature



Thermally stable until maximum operation range(1,8 V)

Negative temperature range of VT: - 2 bis -4 mV / K

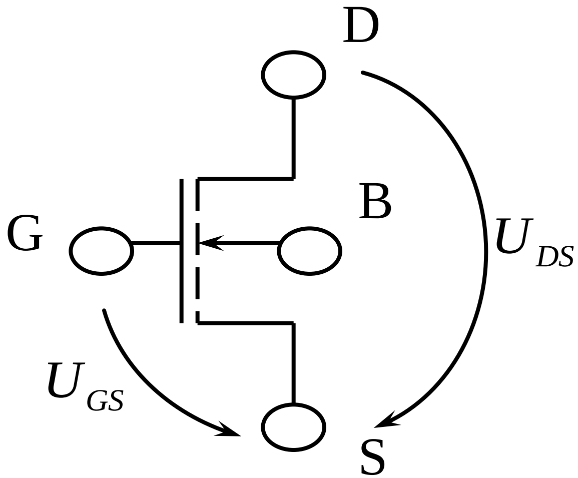
Current equations of MOS-Transistor (1)



off region

$$U_{GS} < U_T \qquad I_D = 0$$

(or nearly zero)



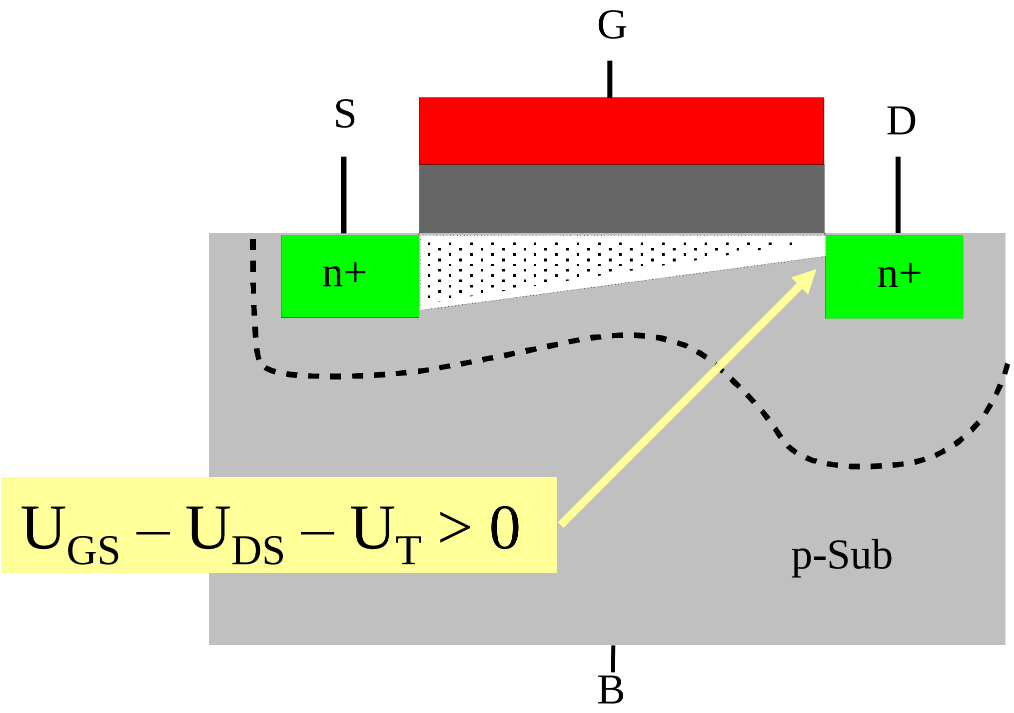
Current equations of MOS-Transistor (2)

Conduction mode

$$U_{GS} > U_T$$

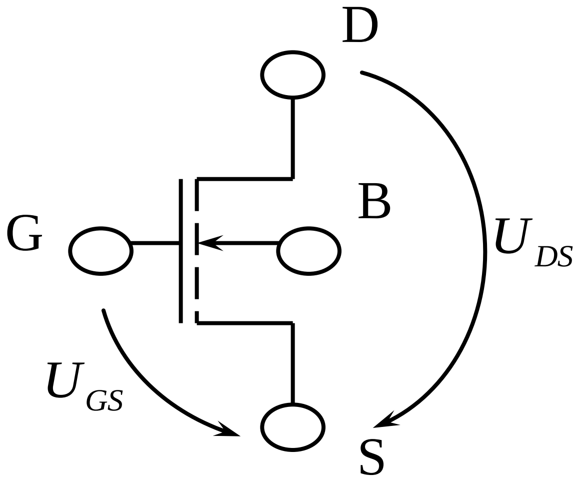
(1) Linear region
(Triode region)

$$U_{DS} < U_{GS} - U_T$$



$$I_D = \beta (U_{GS} - U_T - \frac{1}{2} U_{DS}) U_{DS}$$

$$\beta = \frac{W}{L} \cdot \frac{\mu_n \cdot \varepsilon_{ox}}{t_{ox}} = \frac{W}{L} \cdot \beta_o$$

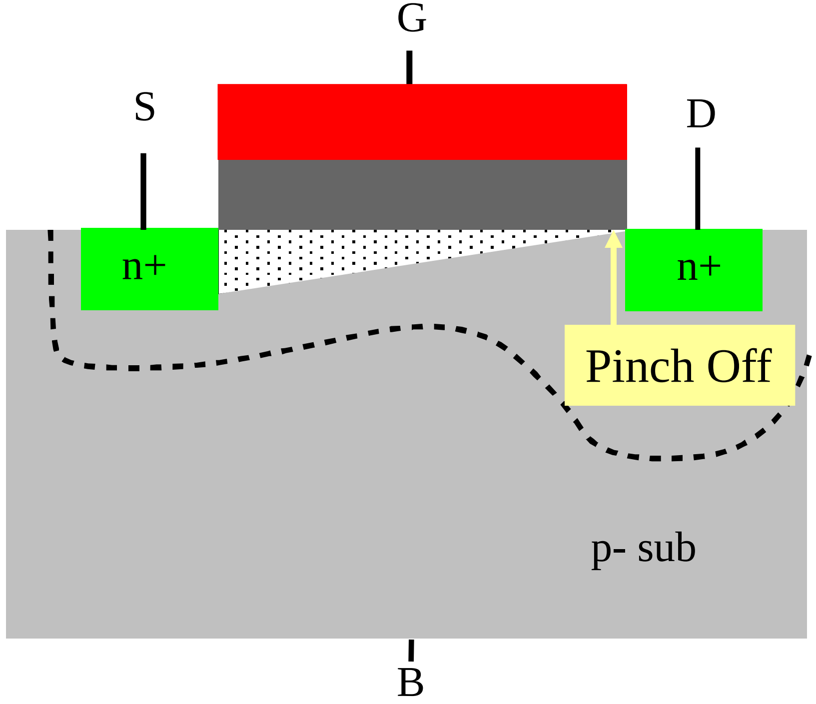


Current equations of MOS-Transistor (3)

(2) Saturation region

$$U_{GS} > U_T$$

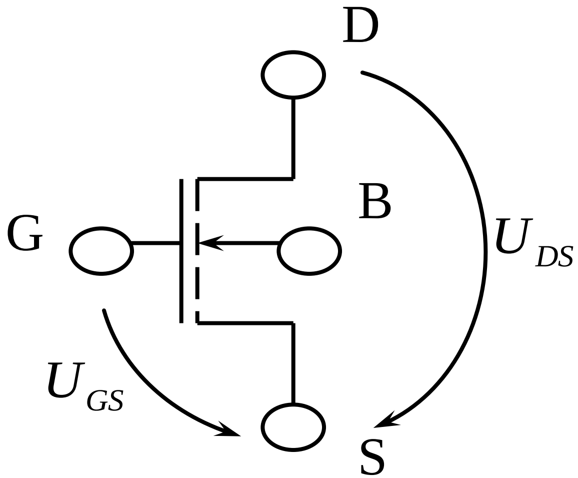
$$U_{DS} > U_{GS} - U_T$$



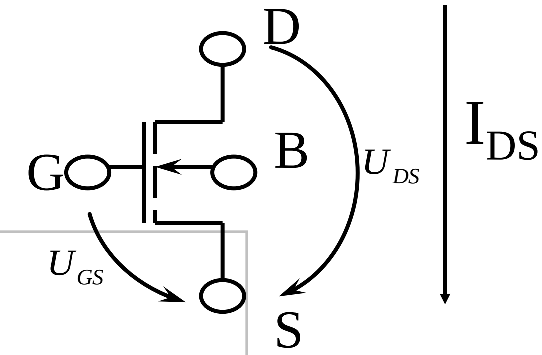
Pinch-off limit

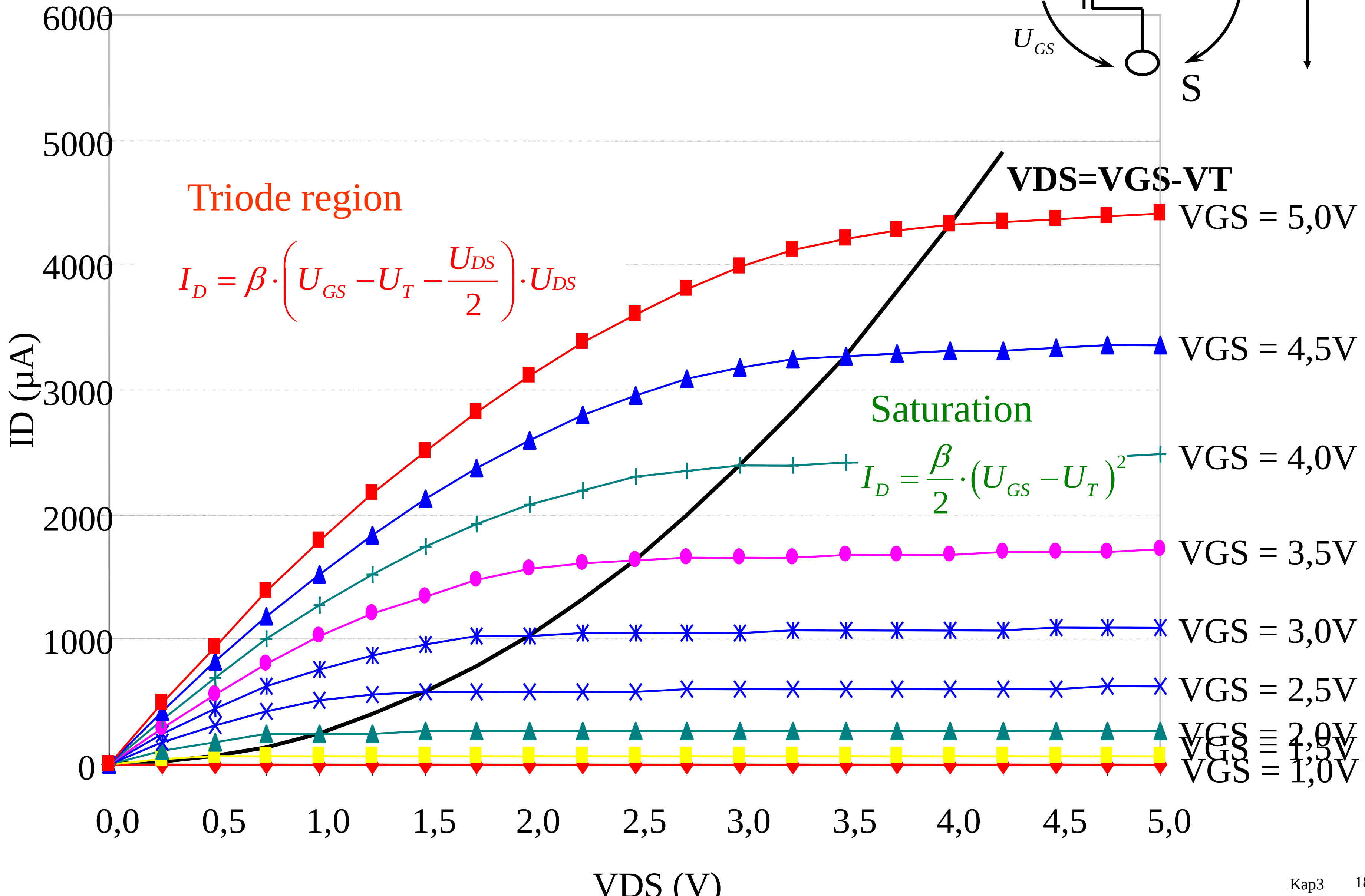
$$U_{DS} = U_{GS} - U_T$$

$$I_D = \frac{\beta}{2}(U_{GS} - U_T)^2$$



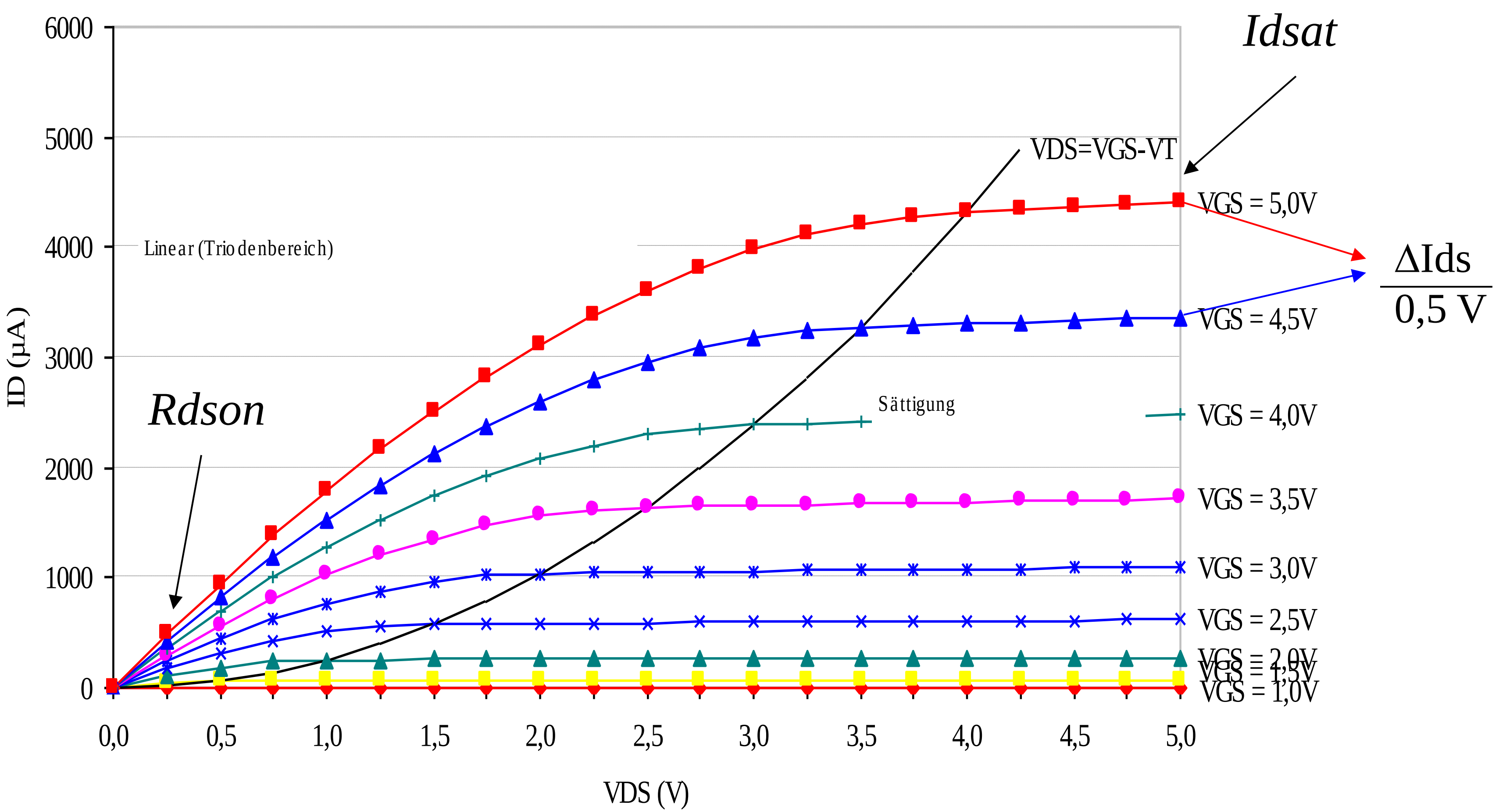
Output characteristics



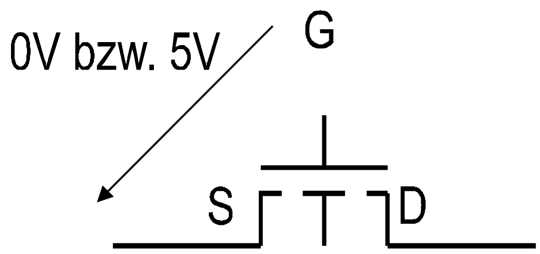


Features of MOS Transistors
(**P**rocess **C**ontrol **M**onitor PCM parameters)

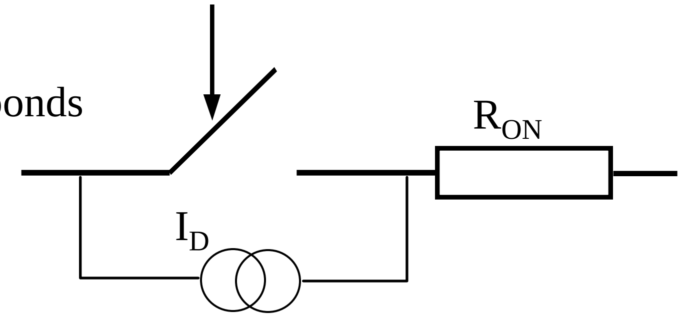
1) Threshold voltage Vt
2) Transconductance Gm (ΔIds/ΔVgs)
3) Saturation current Idsat (with nominal Gate-voltage)
4) Rdson (with nominal Gate-voltage, small Vds)



Current at weak inversion (Subthreshold)



corresponds

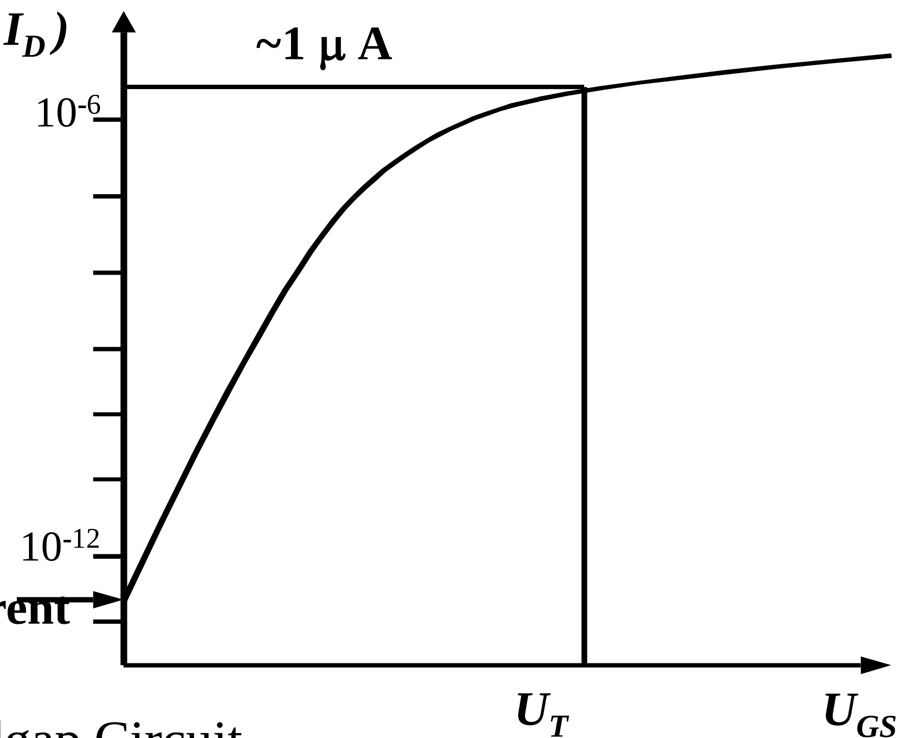


Off region

$$U_{GS} < U_T \qquad I_D = 0\ ?$$

$$I_D = I_{D0} \cdot e^{\left(\frac{U_{GS} - U_T}{nkT/q}\right)}$$

Correlates with
Carrier density on Source

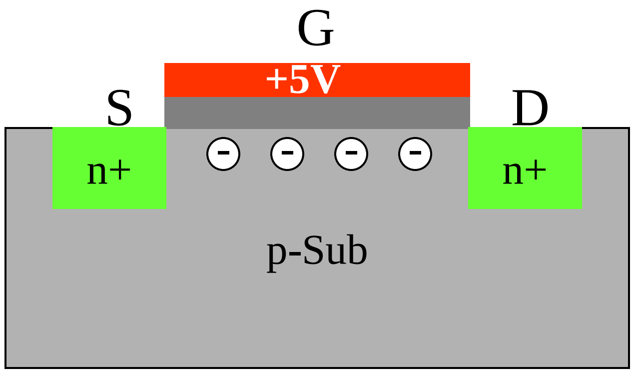


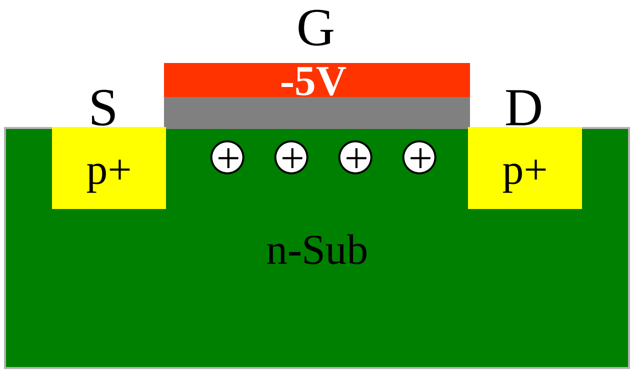
This Bipolar Effect is useful in Bandgap Circuit

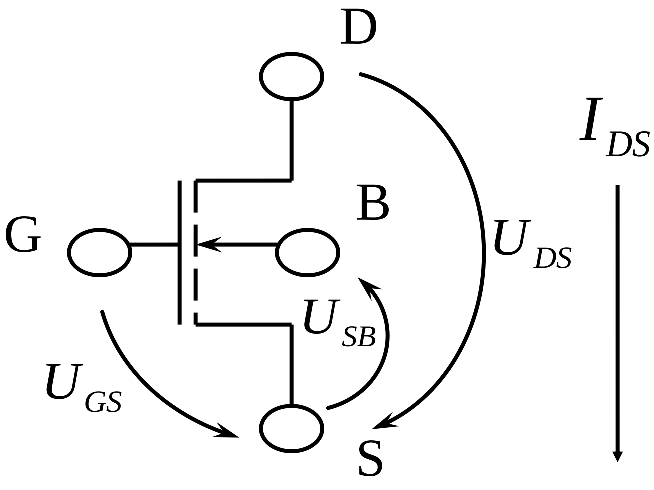
The leakage current may discharge the battery of a mobile device.

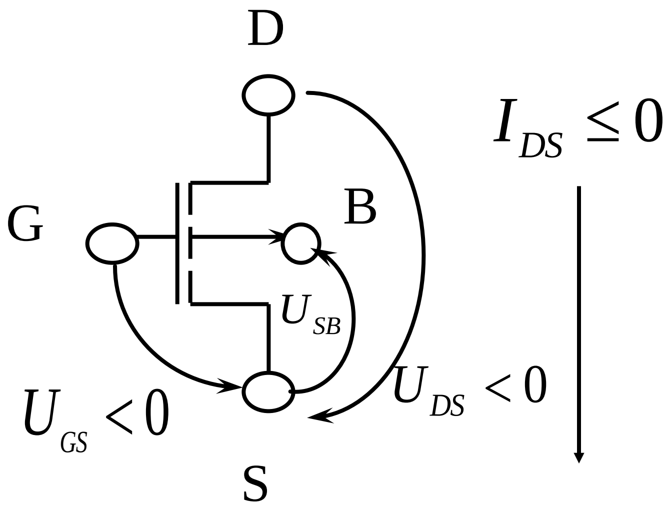
n-Channel-Transistor

p-Channel-Transistor

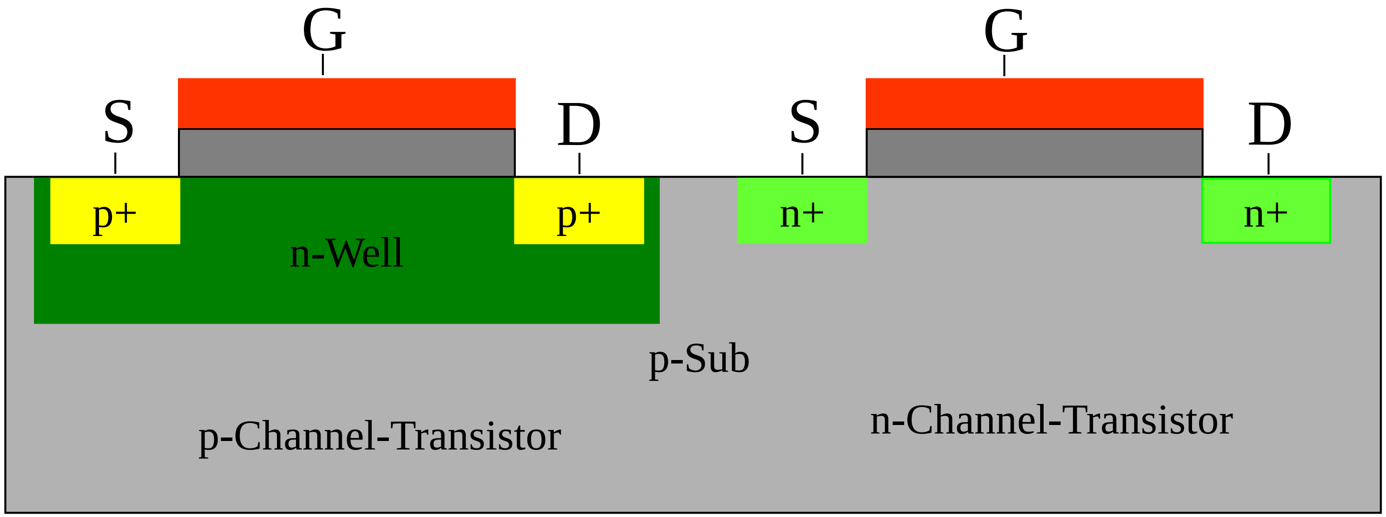


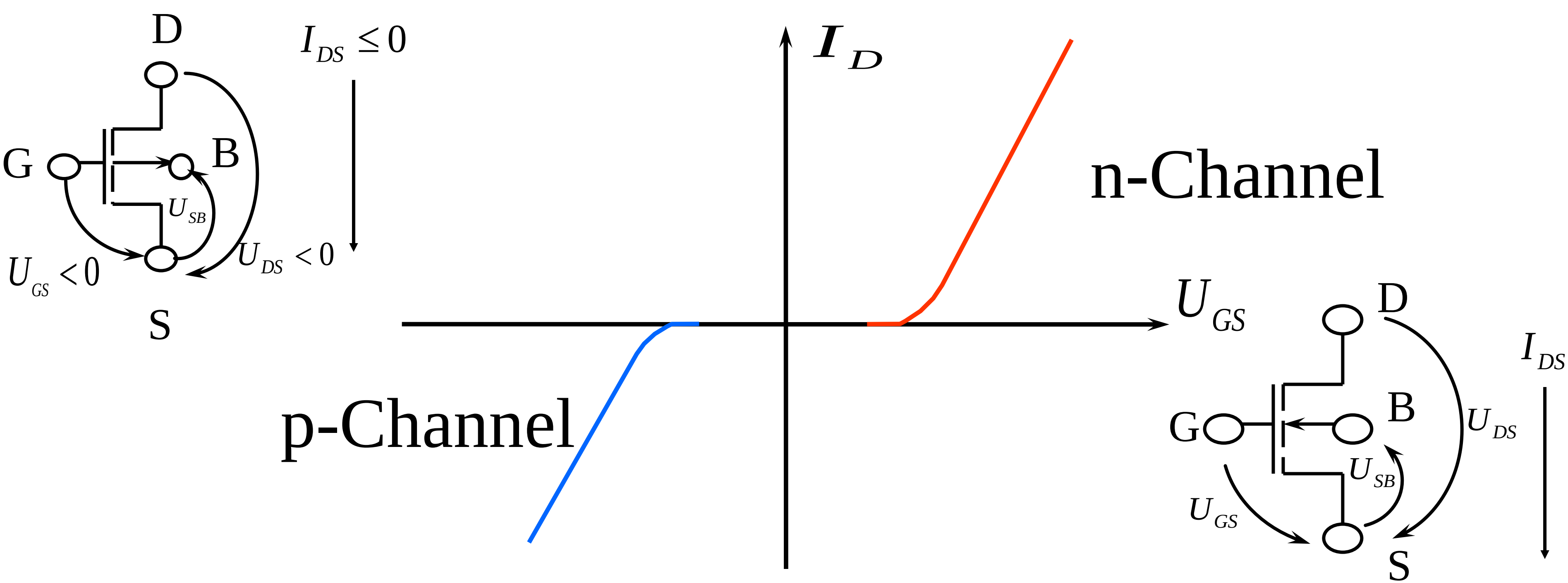




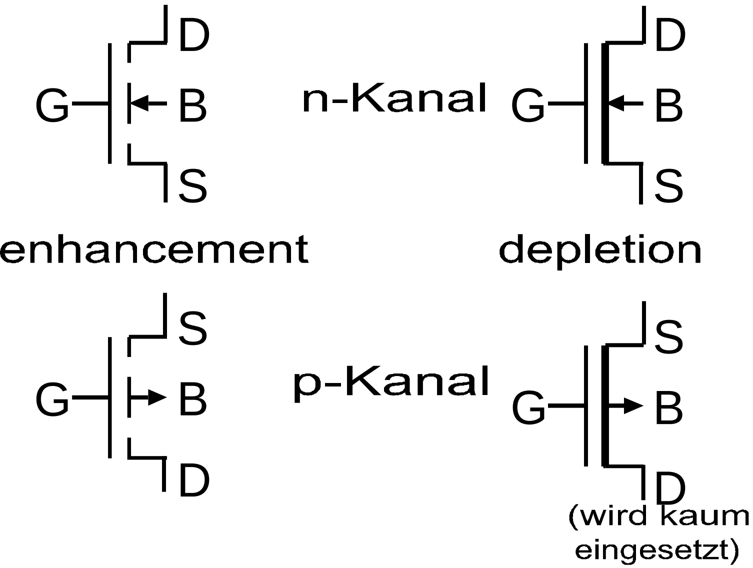


Complementary Metal-Oxide-Semiconductor (CMOS)

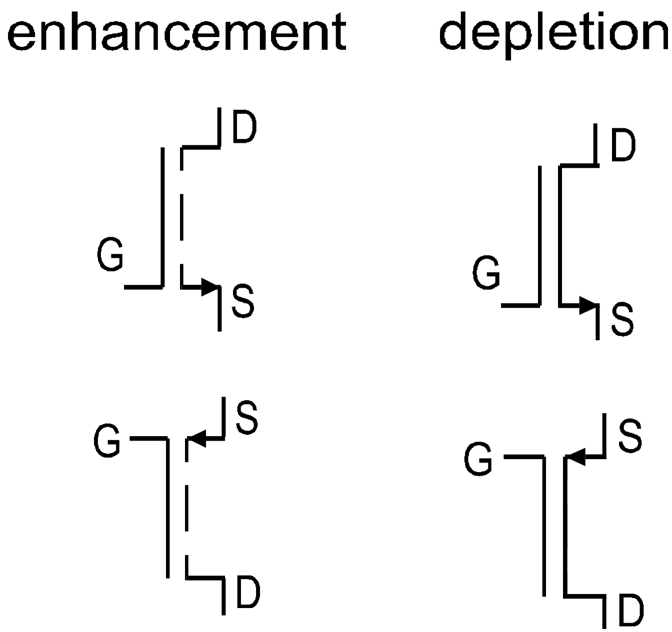




Schematic symbols for MOS-Transistor



Or



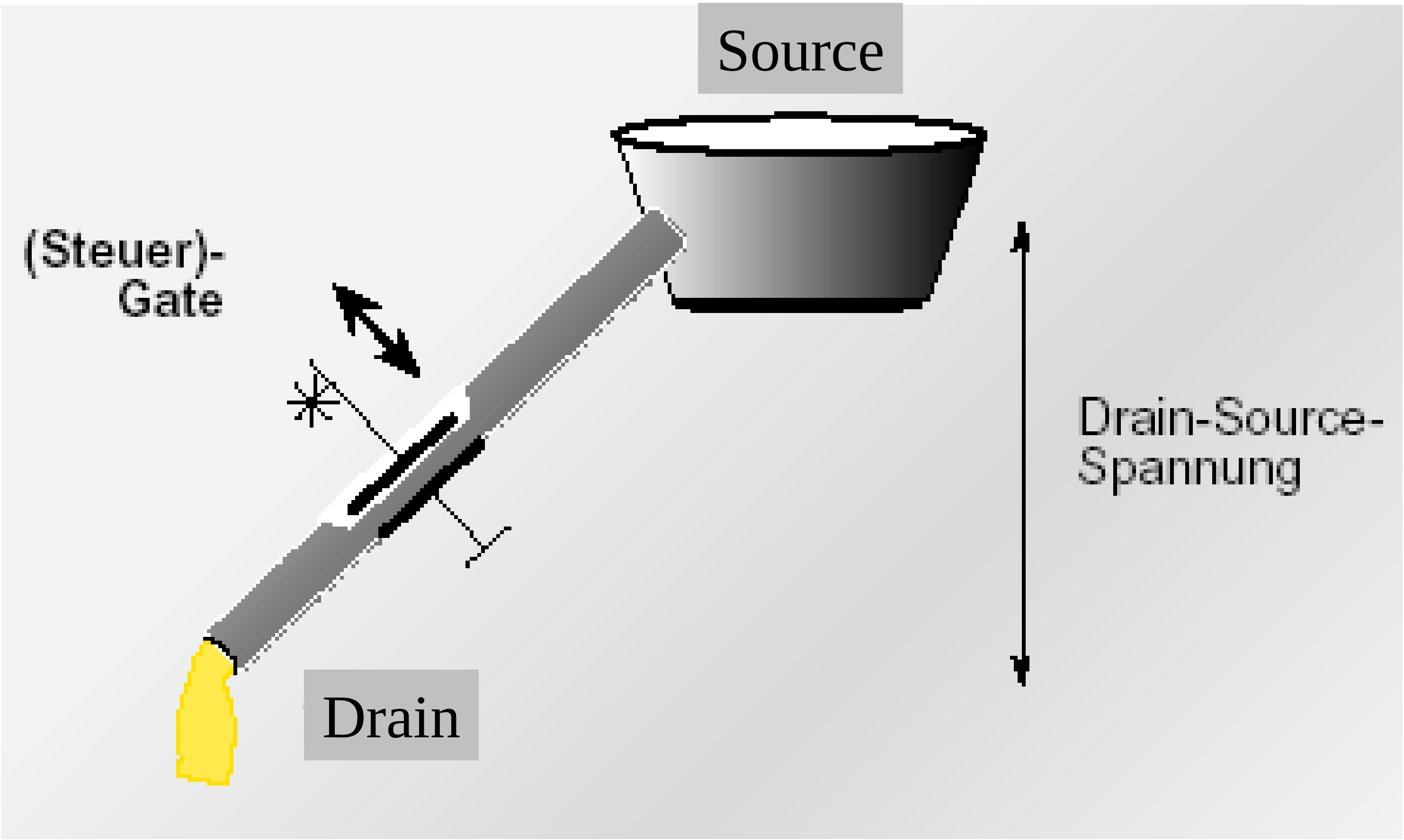
NMOS-Bulk: inward arrowhead, PMOS-Bulk: outward arrowhead

Enhancement: Drain-Source diconnected, three lines for Drain, Bulk and Source
Depletion: Drain-Source connected

PMOS in Schematics:

Source has the highest potential, Current (holes) flows from Source to Drain
Gate high: Transistor off, Gate low: Transistor on

MOSFET Model (Garden hose)



Current:

NMOS: Electrons / PMOS: Holes

What is wrong?