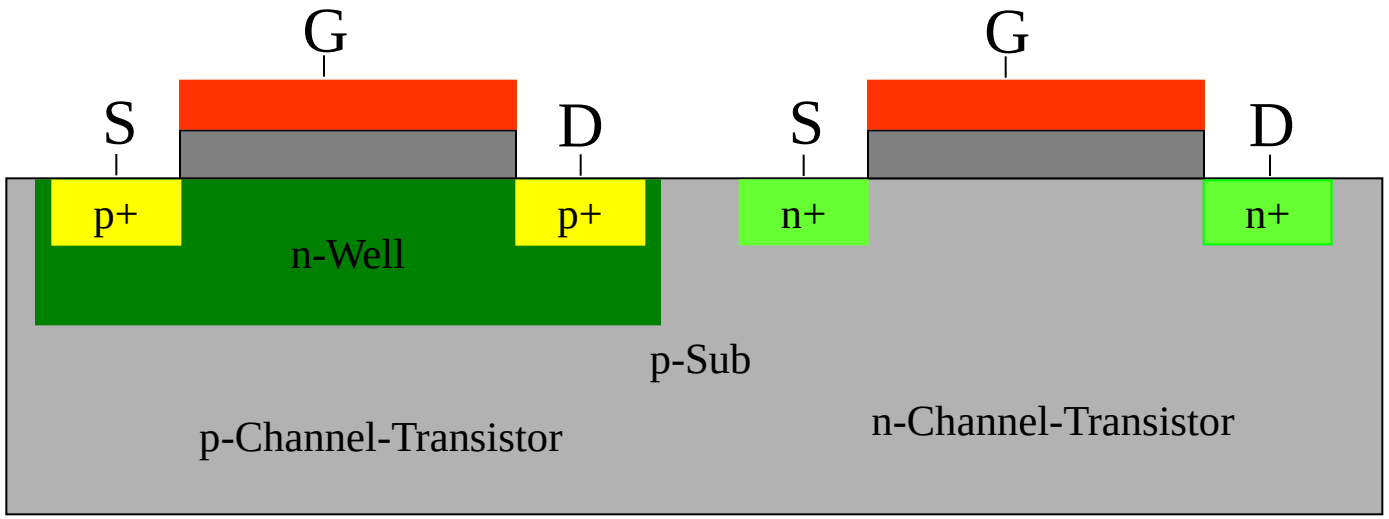
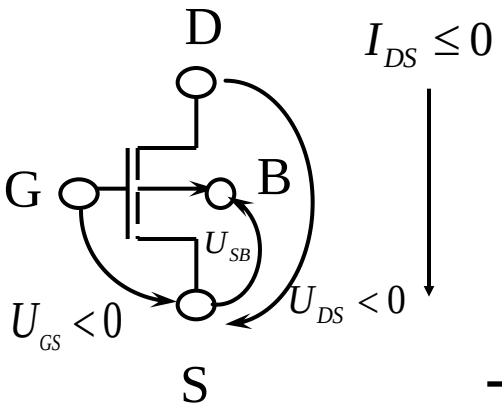
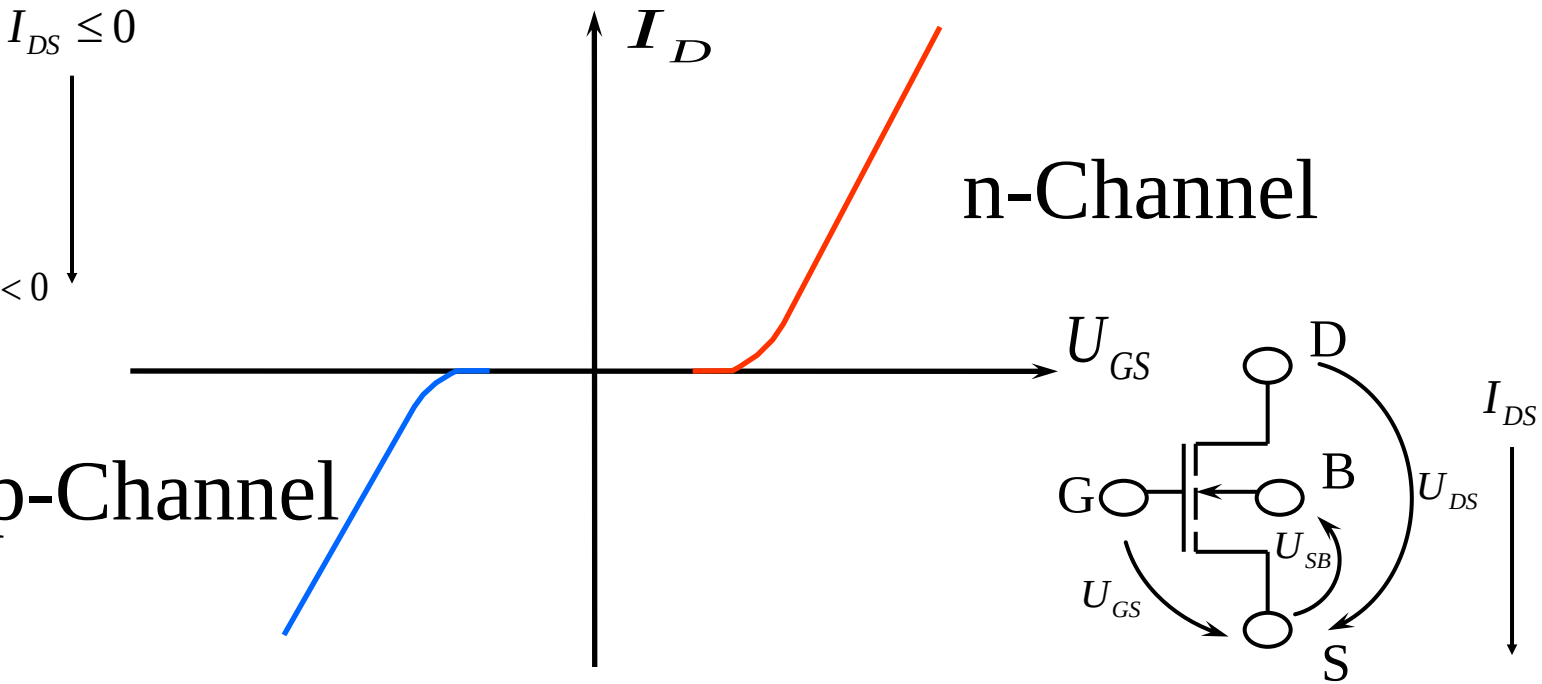
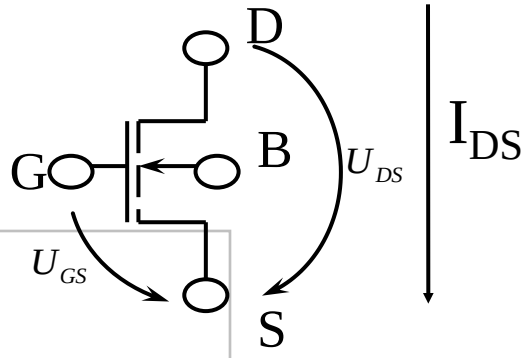
Complementary Metal-Oxide-Semiconductor (CMOS)







Output Characteristics



Triode region

$$I_D = \beta \cdot \left(U_{GS} - U_T - \frac{U_{DS}}{2} \right) \cdot U_{DS}$$

Saturation

$$I_D = \frac{\beta}{2} \cdot (U_{GS} - U_T)^2$$

VDS=VGS-VT

VGS = 5,0V

VGS = 4,5V

VGS = 4,0V

VGS = 3,5V

VGS = 3,0V

VGS = 2,5V

VGS = 2,0V

VGS = 1,5V

VGS = 1,0V

ID (µA)

6000
5000
4000
3000
2000
1000
0

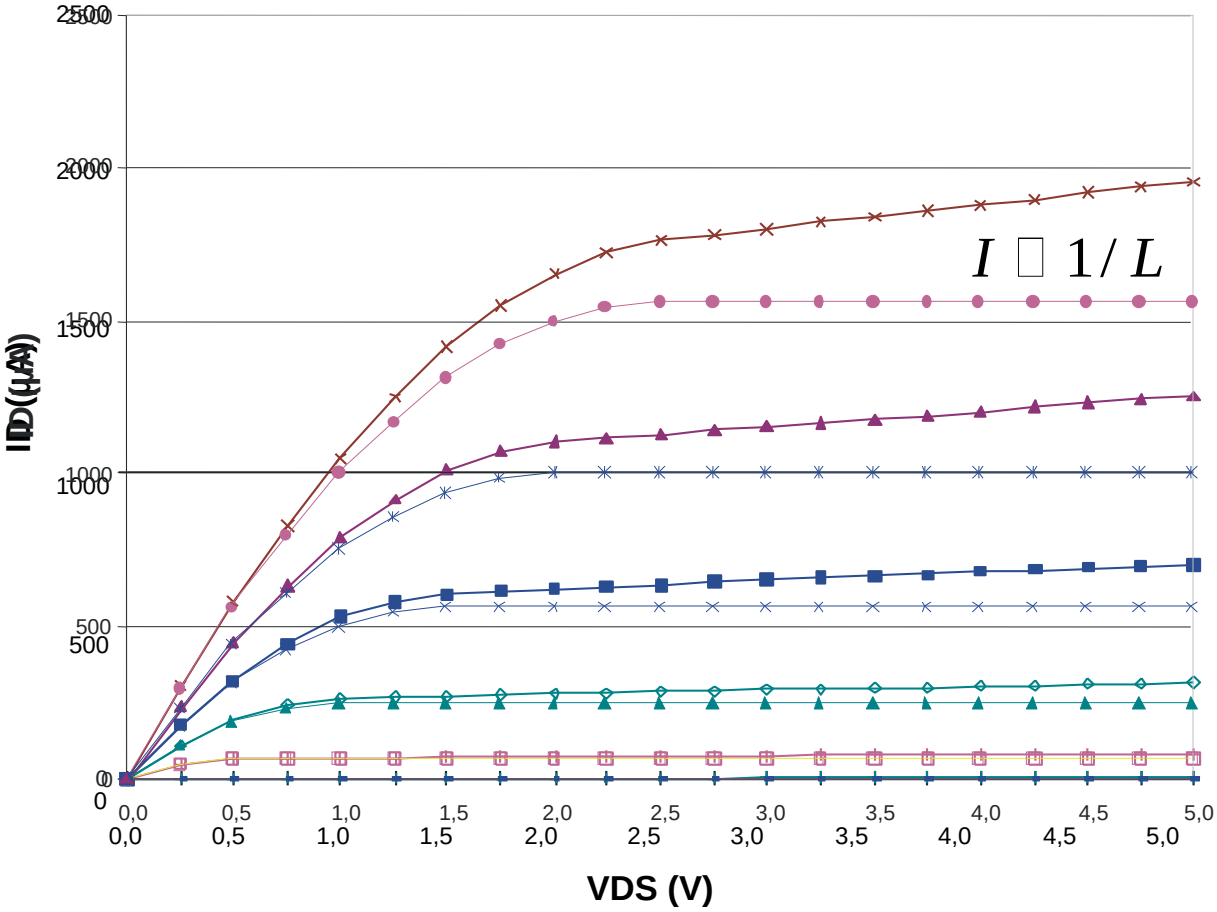
0,0 0,5 1,0 1,5 2,0 2,5 3,0 3,5 4,0 4,5 5,0

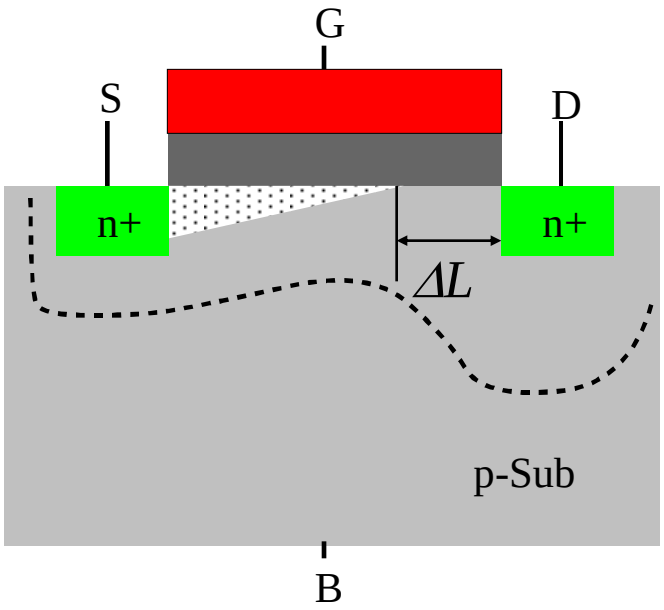
VDS (V)

Further effects and elements of MOSFET

- Channel length modulation
- Short channel effect Vt = f(L , W)
- Effective channel length and width (W / L)
- Capacitances (Gate, Drain, Source)
- Capacitance, resistance in interconnects of a MOS-process
- Parasitic bipolar elements/effects: Diode, Transistor, Latch-up
- Breakdown
- Degradation

Modulation of channel length (1)





Comparison of output characteristics with λ=0 und λ>0

$$I_D = \frac{\beta}{2}(U_{GS} - U_T)^2(1 + \lambda U_{DS})$$

1 / λ corresponds to early-voltage of bipolar transistor

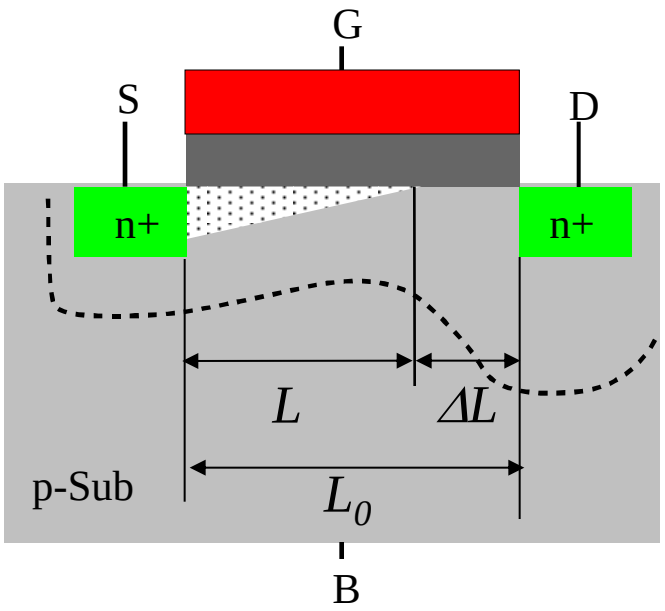
Modulation of channel length (2)

Physical Calculation Model

$$I_D = \frac{W}{L} \cdot \frac{\beta_O}{2} (U_{GS} - U_T)^2 = \frac{L_O}{L} \cdot I_O$$

$$I_D = \frac{L_O}{L_O - \Delta L} \cdot I_O \approx (1 + \frac{\Delta L}{L_O}) \cdot I_O$$

$$\Delta L = k_2 \cdot \sqrt{U_{DS} - U_{DSS}}$$

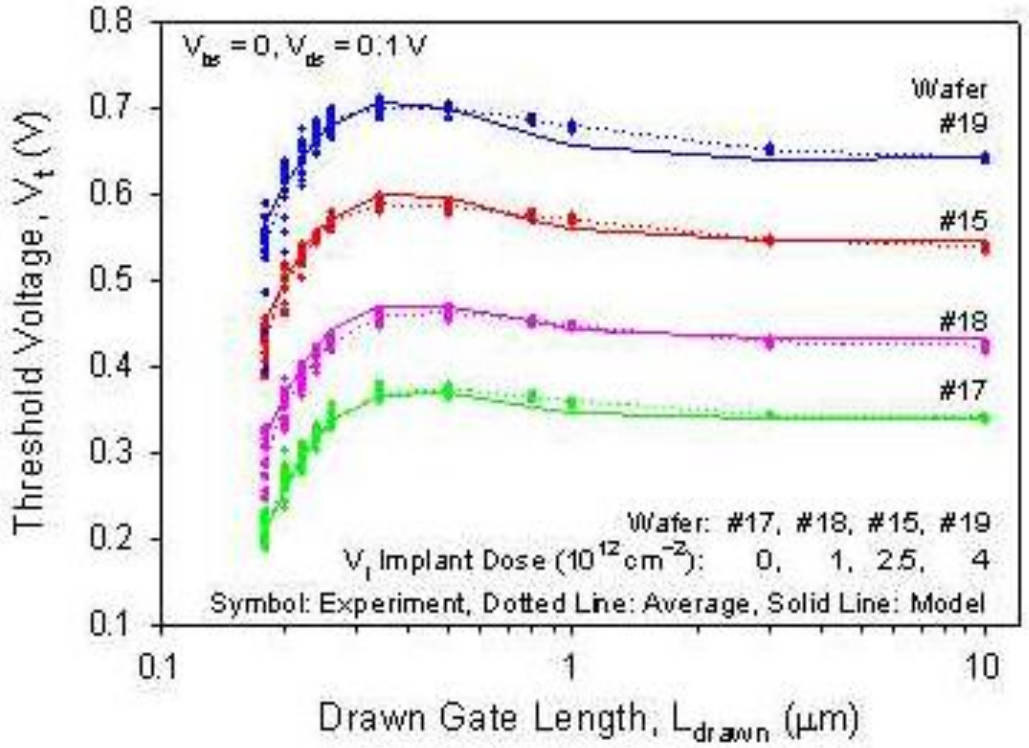


k_2: Factor for the width of space-charge region, U_{DSS}: pinch-off voltage $\Rightarrow U_{GSeff}$

$$g_{DS} = \frac{dI_D}{dV_{DS}} = \frac{k_2 \cdot I_D}{2 \cdot L_O \cdot \sqrt{U_{DS} - U_{DSS}}}$$

The smaller the channel length, the higher g_{DS},
⇨ Less ideal transistor

Short channel effect at threshold voltage

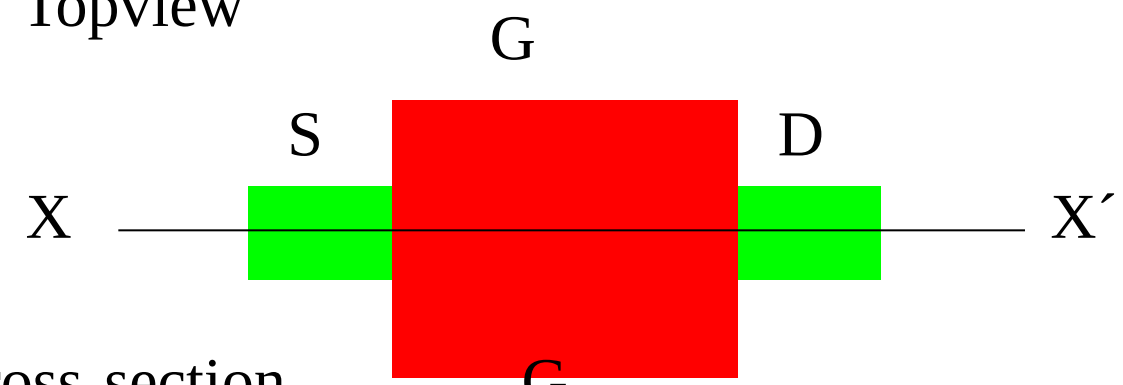


V_T decreases with small channel length for e.g. 100 mV!

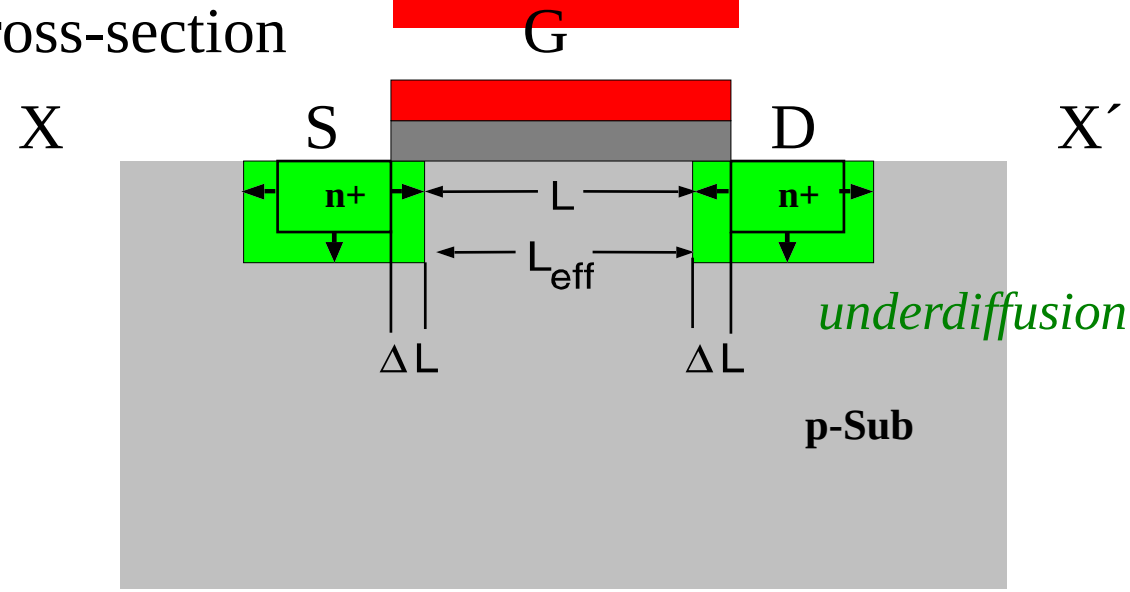
Design of current mirror using narrow channel (w small) is critical, too.

Effective length of Transistor - Underdiffusion

Topview



Cross-section



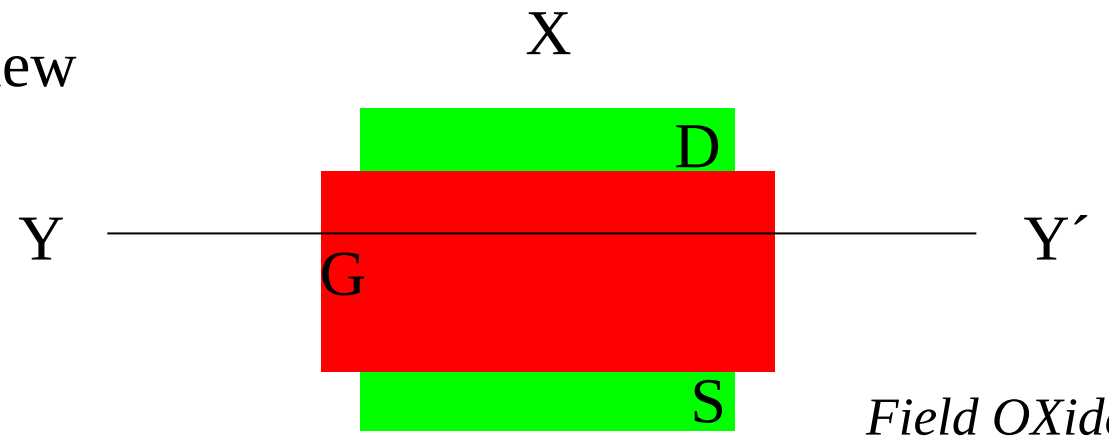
Typical values:
L = 0,35 µm
ΔL = 40 nm
L_{eff} = 0,27 µm

$$L_{eff} = L - 2\Delta L$$

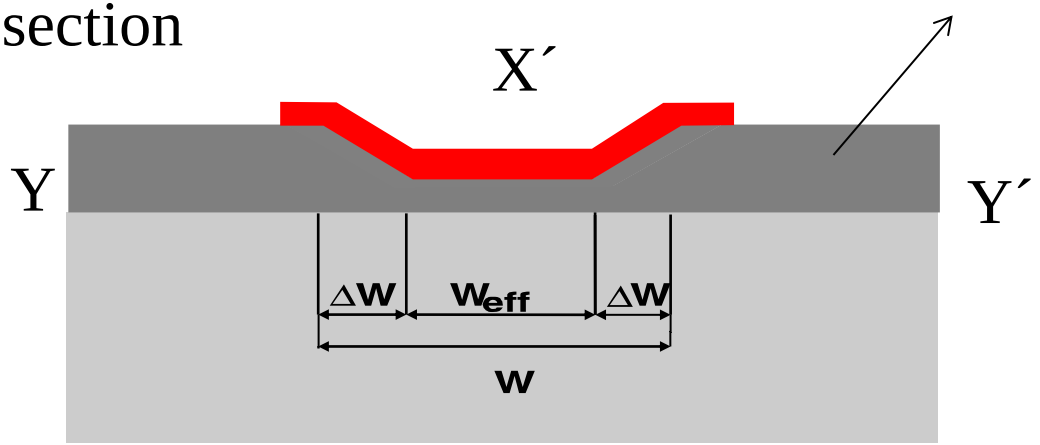
The channel length is defined by the poly gate mask (red)

Effective width of Transistor

Topview



Cross-section

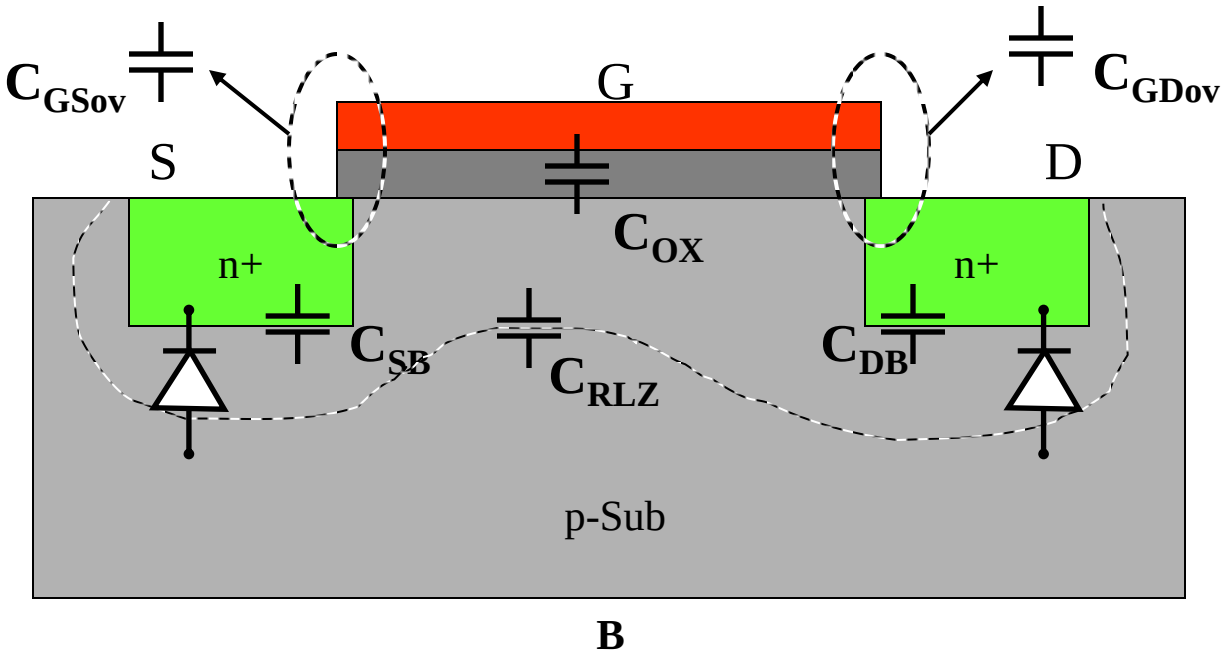


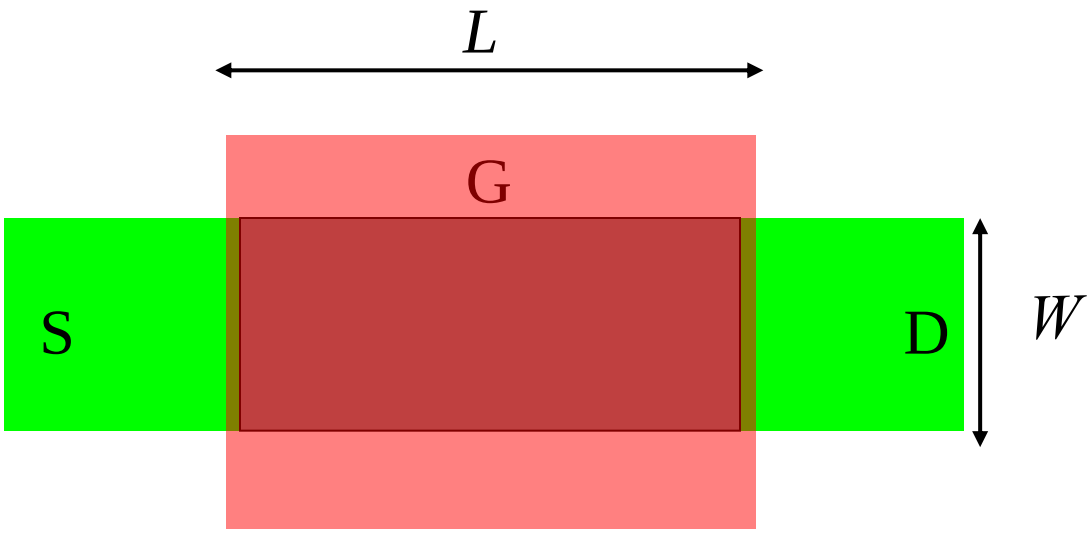
Typical values:
W = 0,5 µm
ΔW = 100 nm
W_{eff} = 0,3 µm

$$W_{eff} = W - 2\Delta W$$

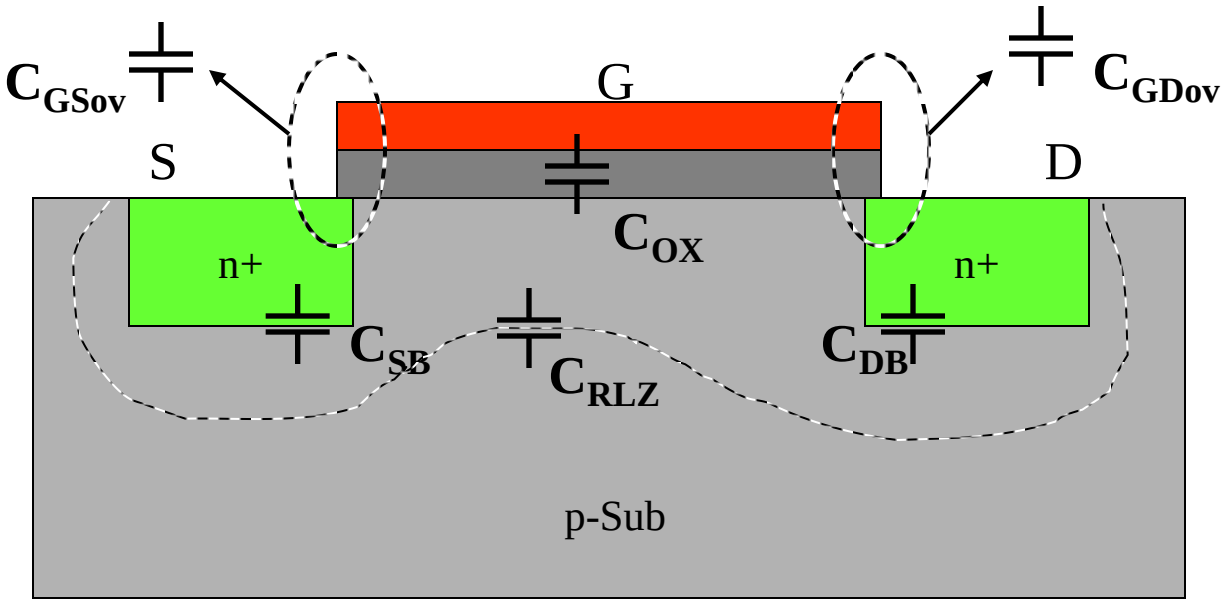
The channel width is defined by the active mask (green)

Parasitic Capacitances of MOS-Transistor





Parasitic Capacitances of MOS-Transistor



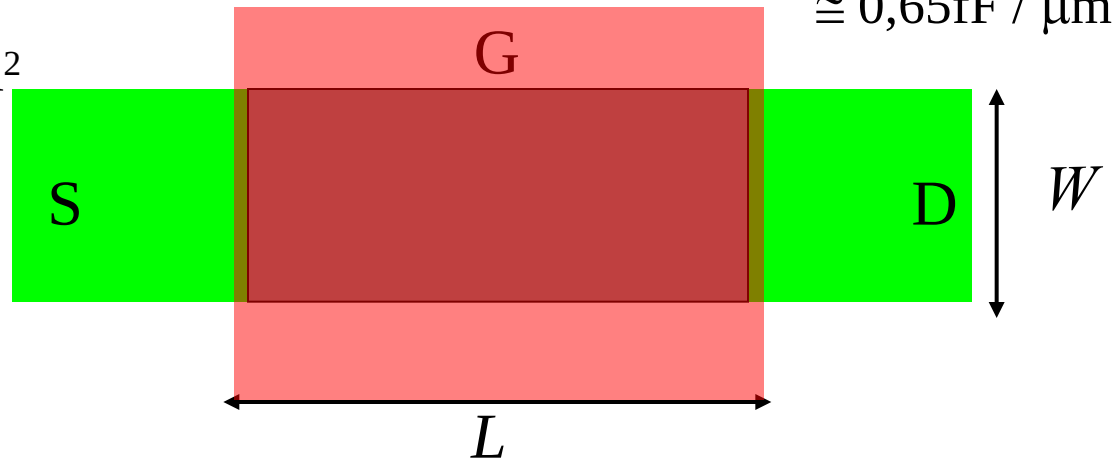
$$C_{OX} = W \cdot L \cdot C'_{OX} = W \cdot L \cdot \frac{\varepsilon_{OX}}{t_{OX}}$$

$$C_{OV} = W \cdot \Delta L \cdot \frac{\varepsilon_{OX}}{t_{OX}}$$

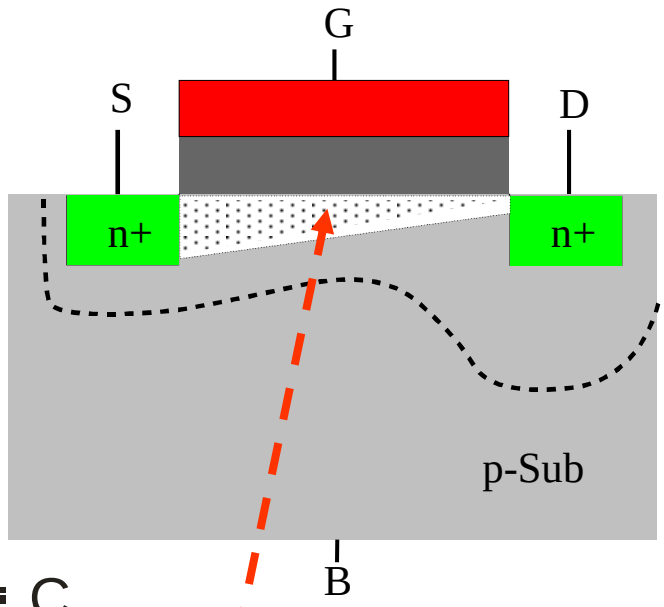
with tox = 10 nm

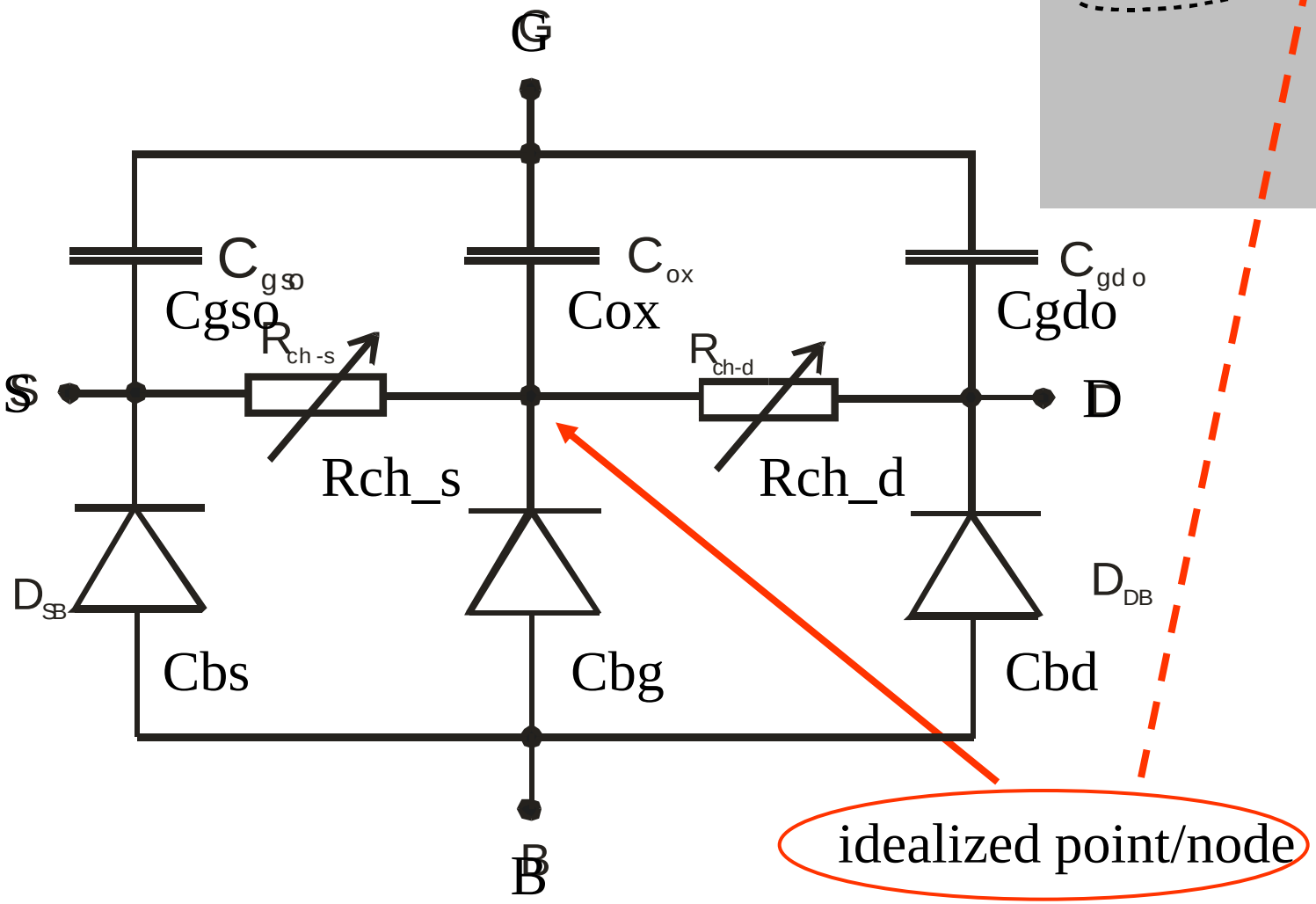
C´ox = 5,7fF / µm²

≅ 0,65fF / µm channel width

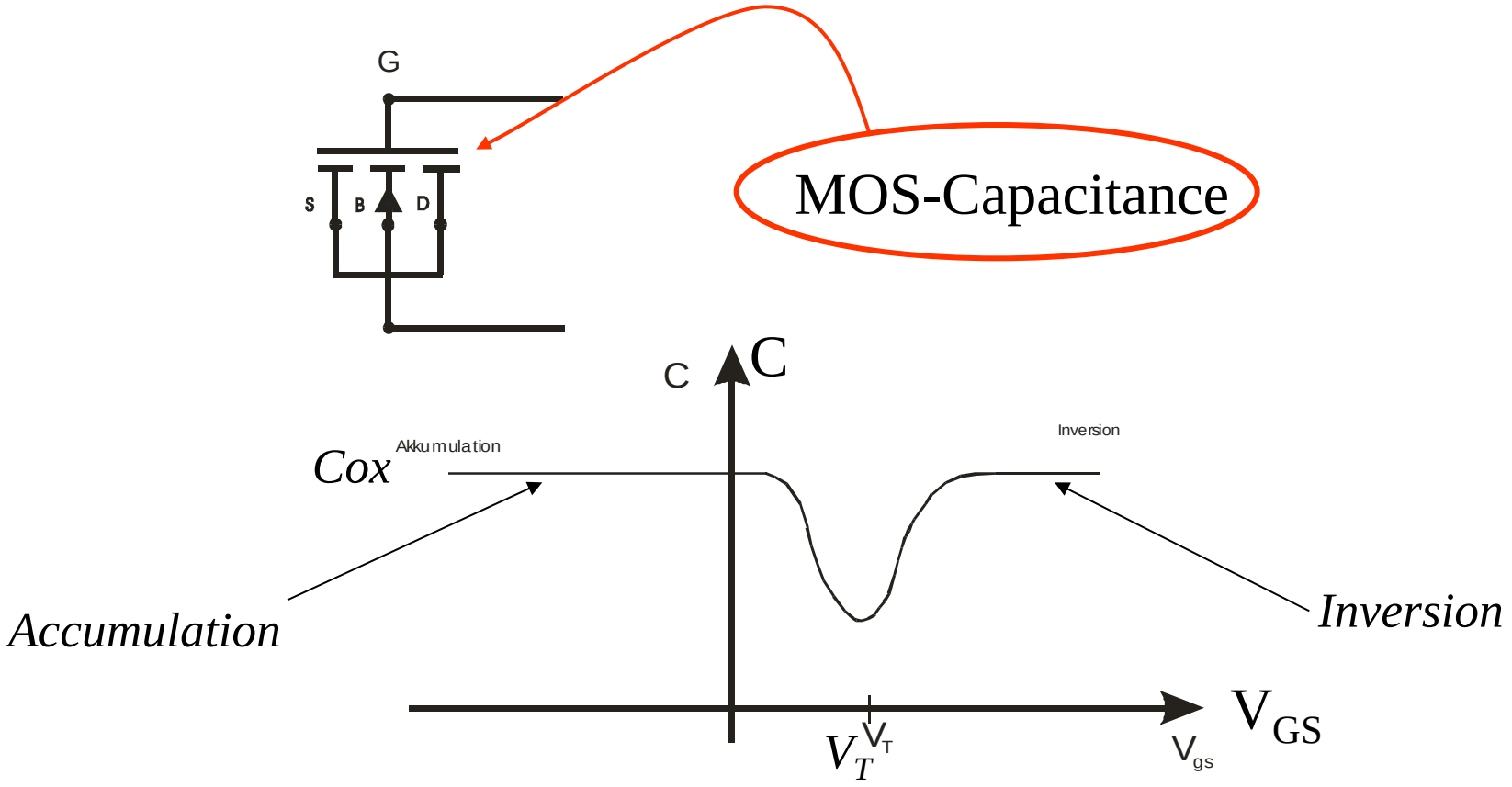


The Capacitance Model





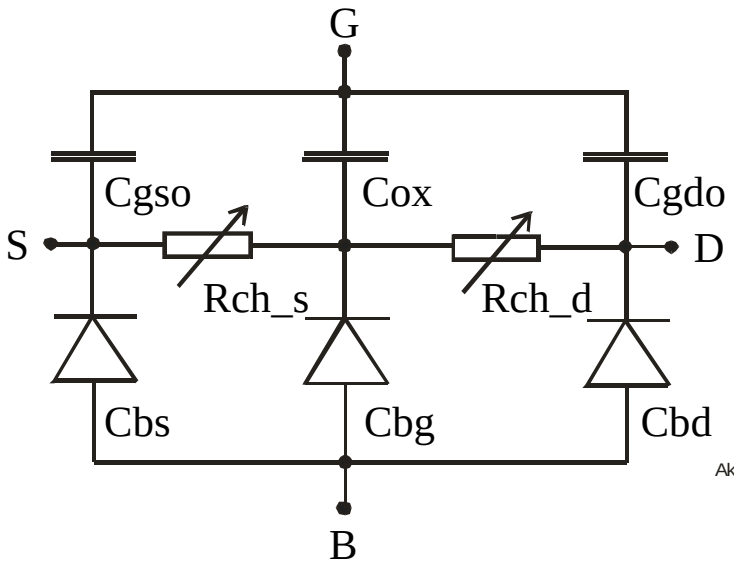
Usage of MOSFET as Capacitance

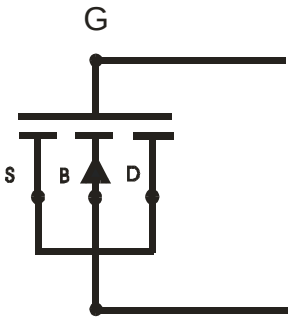


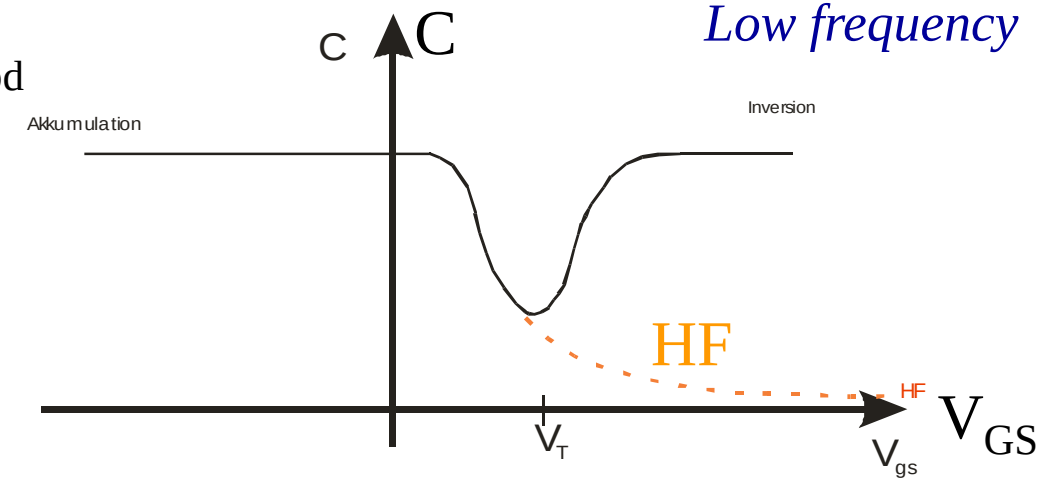
High capacitance due to thin gateoxide.

For Vgs around Vt (between accumulation and inversion) only the depletion capacitance Cbg is effective.

Behaviour of MOS-Capacitance at HF resp. high Dynamics



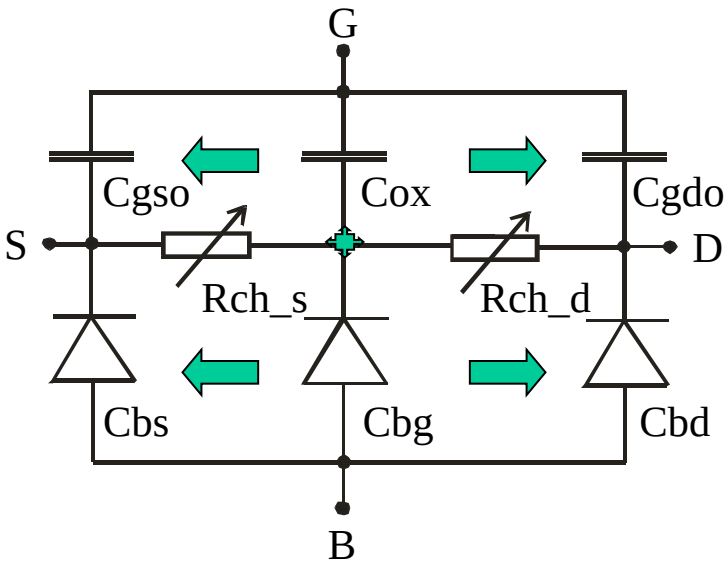




With high frequency/switching speed the channel may not be formed.

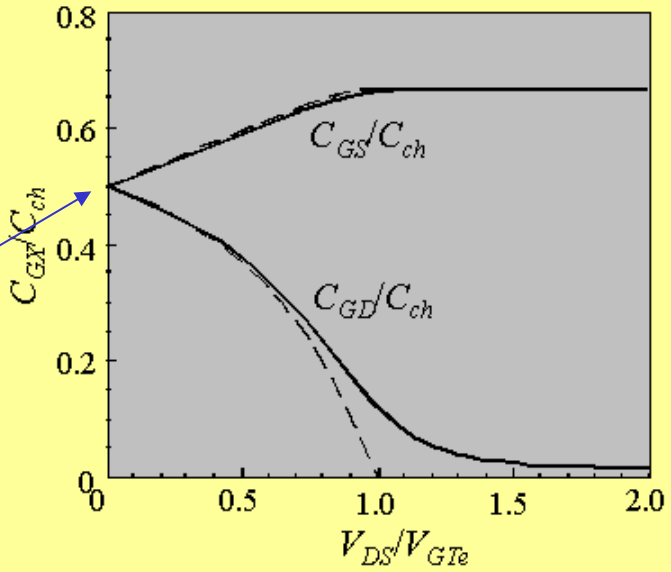
⇨ C_{BG} dominates.

Distribution of Gateoxid-Capacitance between Drain and Source



With Vds = 0
Cgs = Cgd = Cox / 2

Unified Meyer Capacitances III



T. A. Fjeldly, T. Ytterdal, M. S. Shur, *Introduction to Device Modeling and Circuit Simulation*, Wiley, New York , 1998

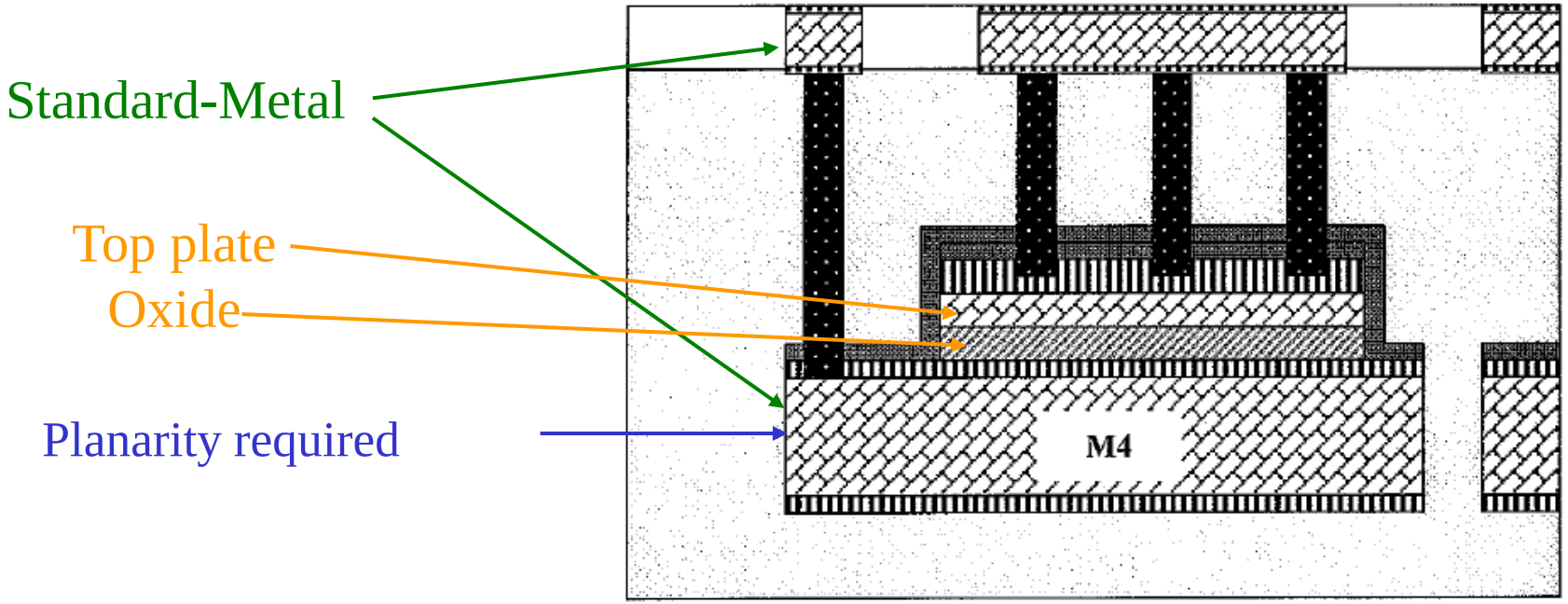
With increasing Vds the part of Cgs grows up to 2/3 of Cox,
as the Rch_d increases.
With large Vds, Cgd is falling to overlap capacitance Cgdo.
Cgd is the feedback capacitance and therefore the most important capacitance.

Further Capacitances in a MOS-Process

For process generation up to 0.25 um two Poly´s may be available.

⇨ Poly-Poly Capacity possible (PiP)

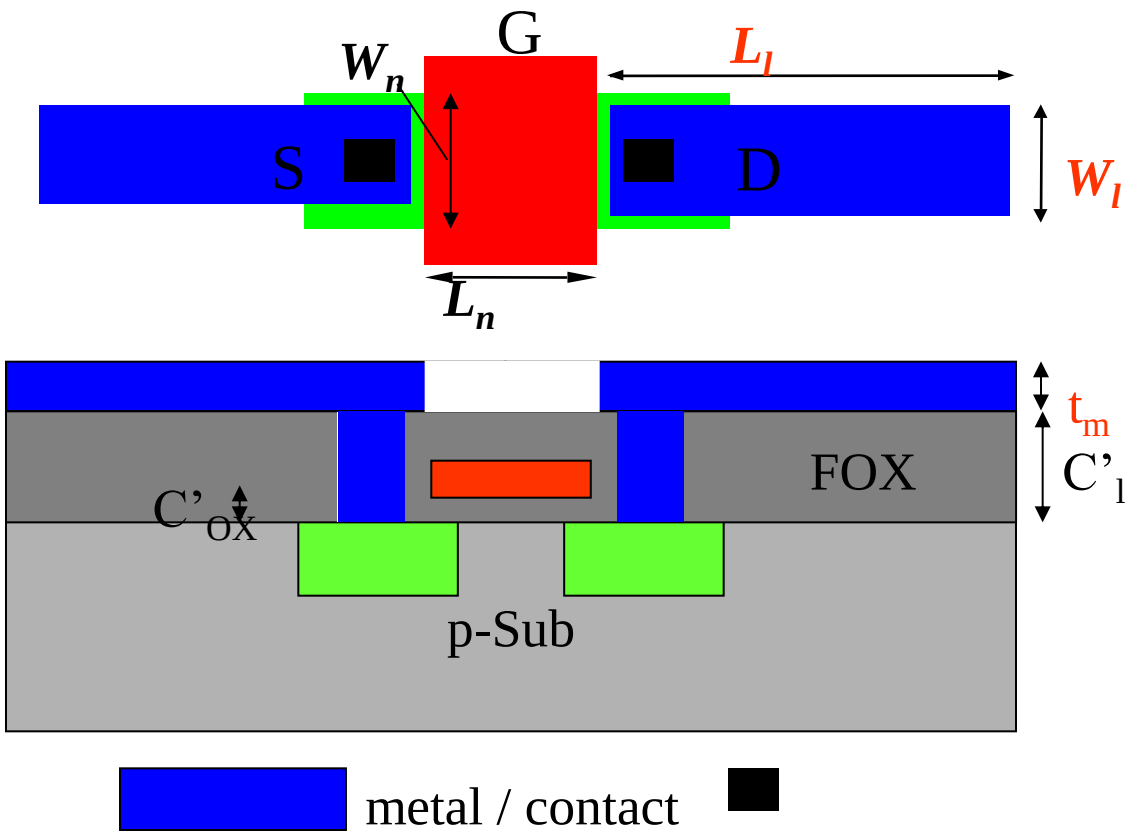
In new processes Metal-Isolator-Metal Capacity (MiM) may be available with a specific thin oxide (e.g. 38 nm) in between.



⇧Advantage: high capacity (e.g.: 1fF/μm^2), high quality

⇩Disadvantage: higher process costs

Interconnect / Lines



$$R = \rho \frac{L_l}{t_m \cdot W_l}$$

$$= \frac{\rho}{t_m} \cdot \frac{L_l}{W_l}$$

$$= \rho_{\square} \cdot \frac{L_l}{W_l}$$

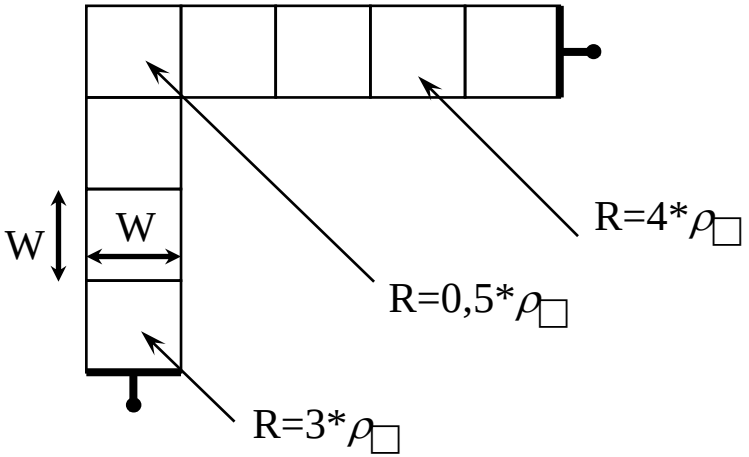
Thickness of line: process parameter, subsequently square (sheet) resistance

(e.g. Metal: 50mΩ/ □ , Poly 20Ω/ □ , N+/P+-resistance 200Ω/ □)

L / W = number of squares: Design / Layout-Parameter

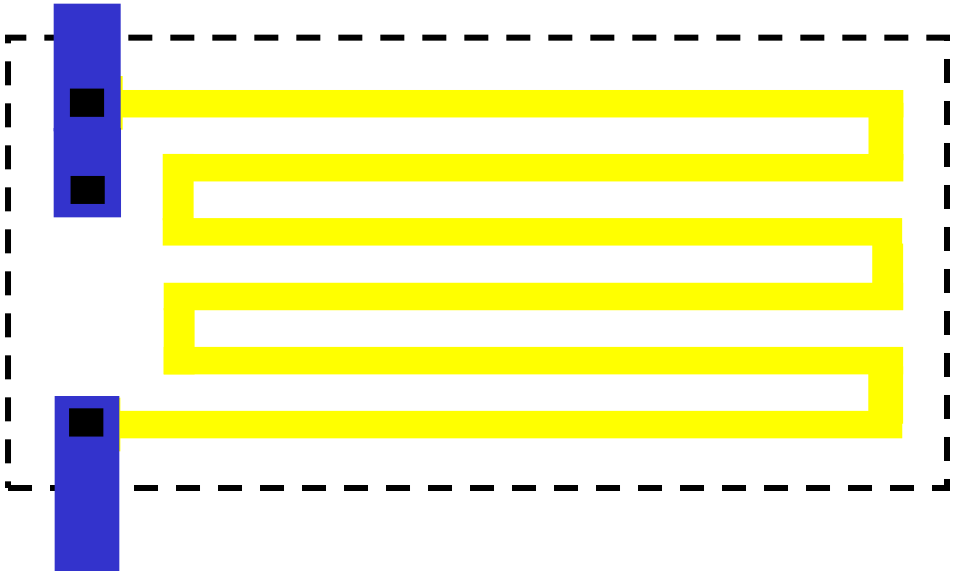
Every contact hole (vias) has also a fixed resistance (e.g. 100 Ω)

Square (Sheet) Resistance

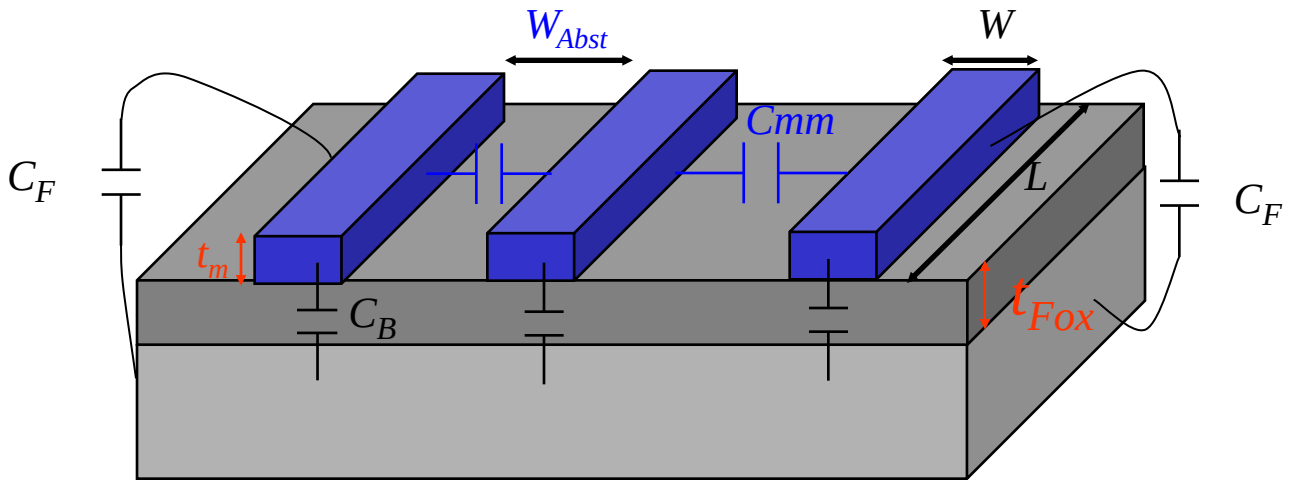


$$R_{ges} = \rho_{\square} * (0.5 \cdot \text{number of corners} + \text{number of 'squares'})$$

Layout example
of a large
resistance with P^+



Line capacitance



$$C_B = W \cdot L \cdot \frac{\varepsilon_{OX}}{t_{FOX}}$$

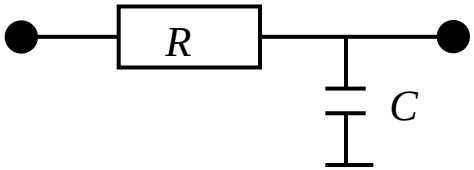
$$C_{mm} = \varepsilon_{OX} \cdot \frac{t_m \cdot L}{W_{Abst}}$$

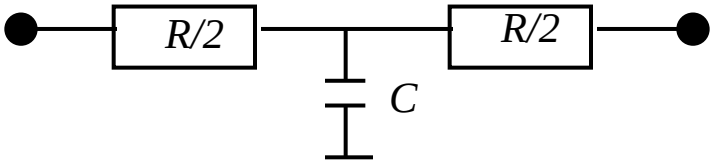
depending on layout

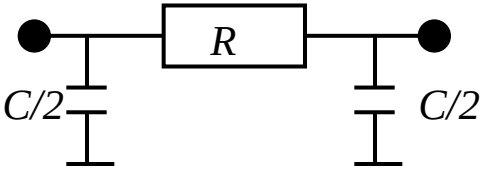
$$C_F \approx \varepsilon_{OX} \cdot \frac{t_m \cdot L}{t_{FOX} + t_m / 2}$$

Typical values: C_B = 10 aF/μm^2, C_F = 4 aF/ μm Perimeter

Equivalent circuit for Interconnect

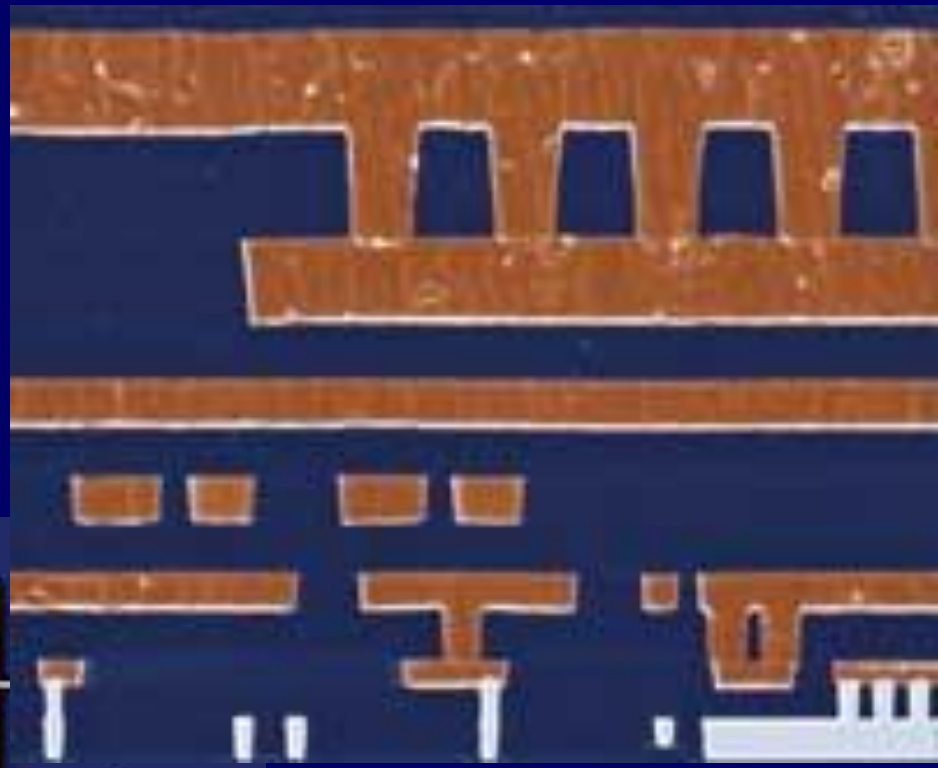


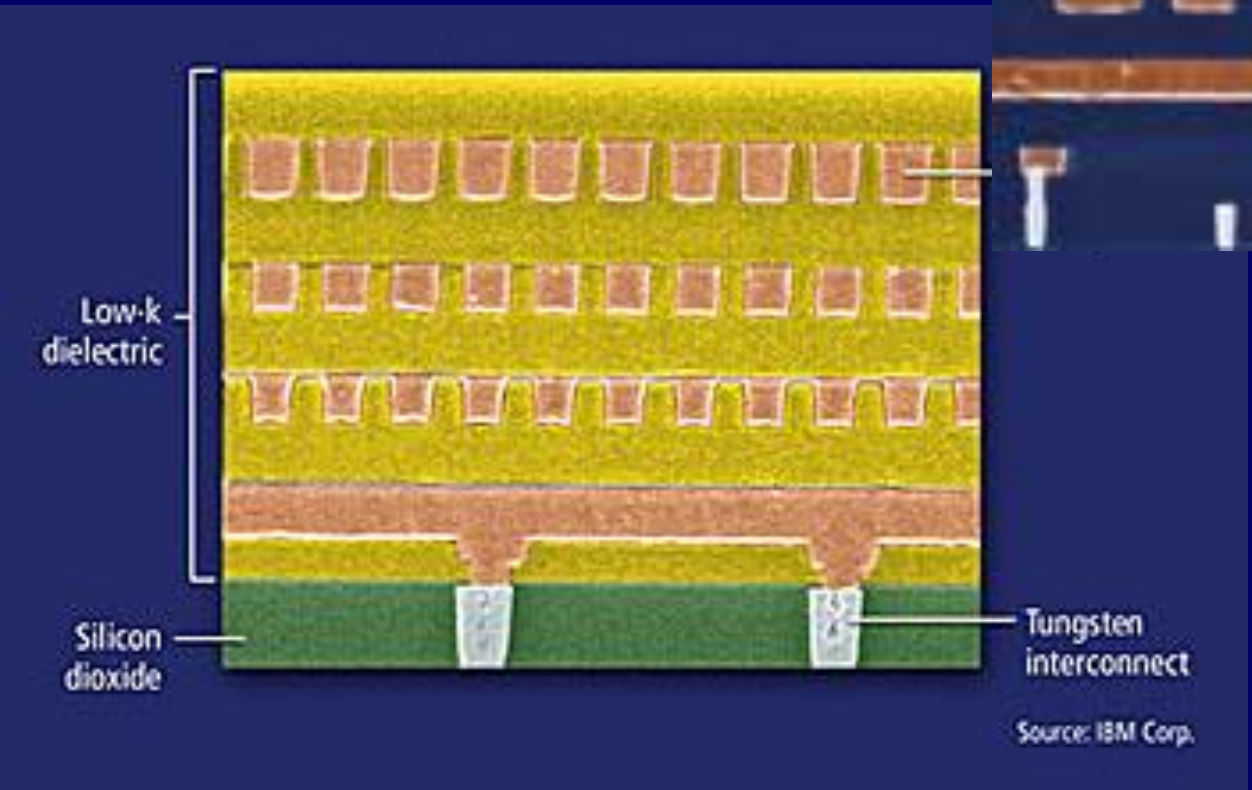




It is possible to connect such a circuit in series
(as known from transmision line theory).

Cross-sections of multilayer-lines

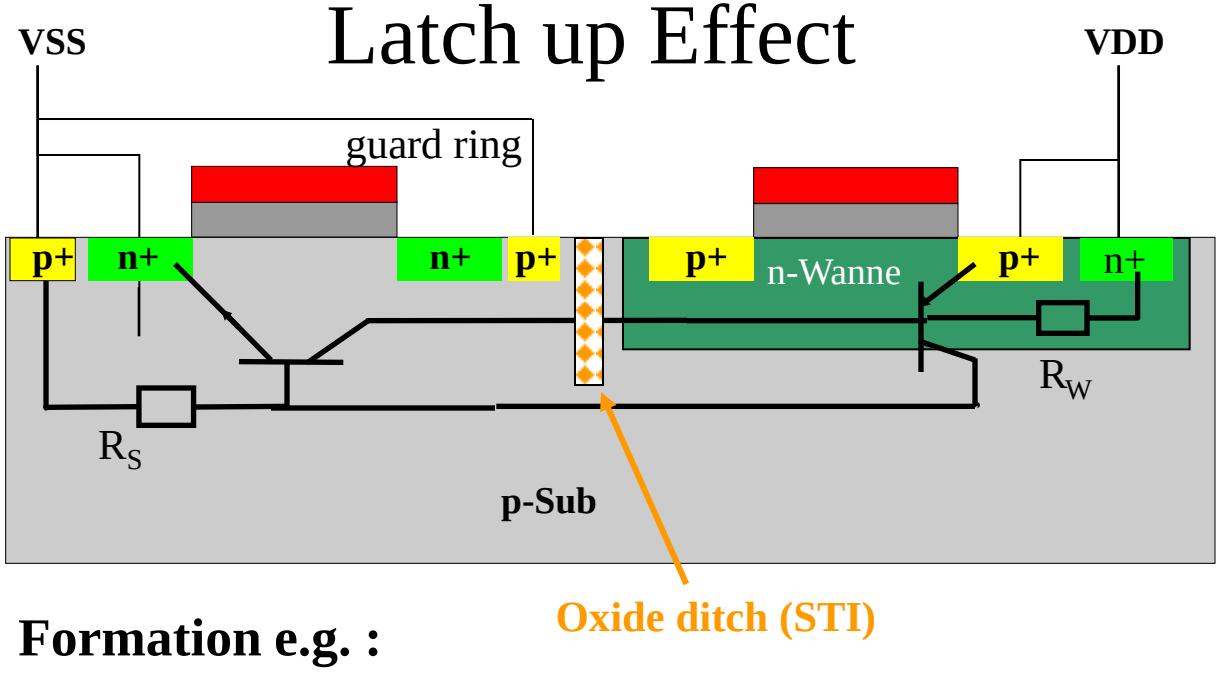


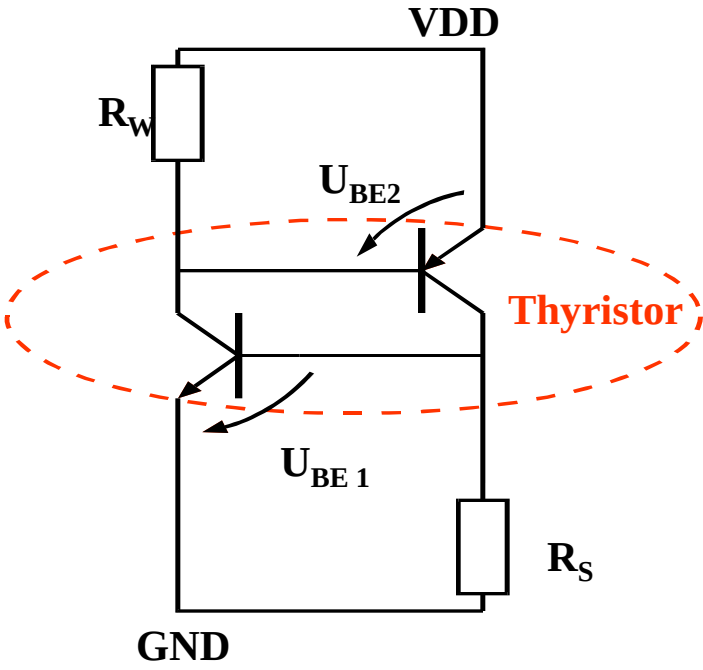


Further Effects and Elements of MOSFET

- Channel length-modulation
- Short channel effect Vt = f(L , W)
- Effective length and width of channel (W / L)
- Capacitances (Gate, Drain, Source)
- Capacitance, resistance and wiring of a MOS-process
- Parasitic bipolare elements/effects: Diode, Transistor, Latch-up
- Breakdown
- Degradation

Latch up Effect





Formation e.g. :

Voltage drop at $R_S \Rightarrow$
U_{BE1} activates BE1 diode $\Rightarrow$
Voltage drop due to
collector current at $R_W \Rightarrow$
U_{BE2} activates BE2 diode $\Rightarrow$
Voltage drop at R_S

Root Causes e.g. :

Spikes of supply voltages
overshoot of Vdd,
undershoot of Vss/ground
(Input, output driver)

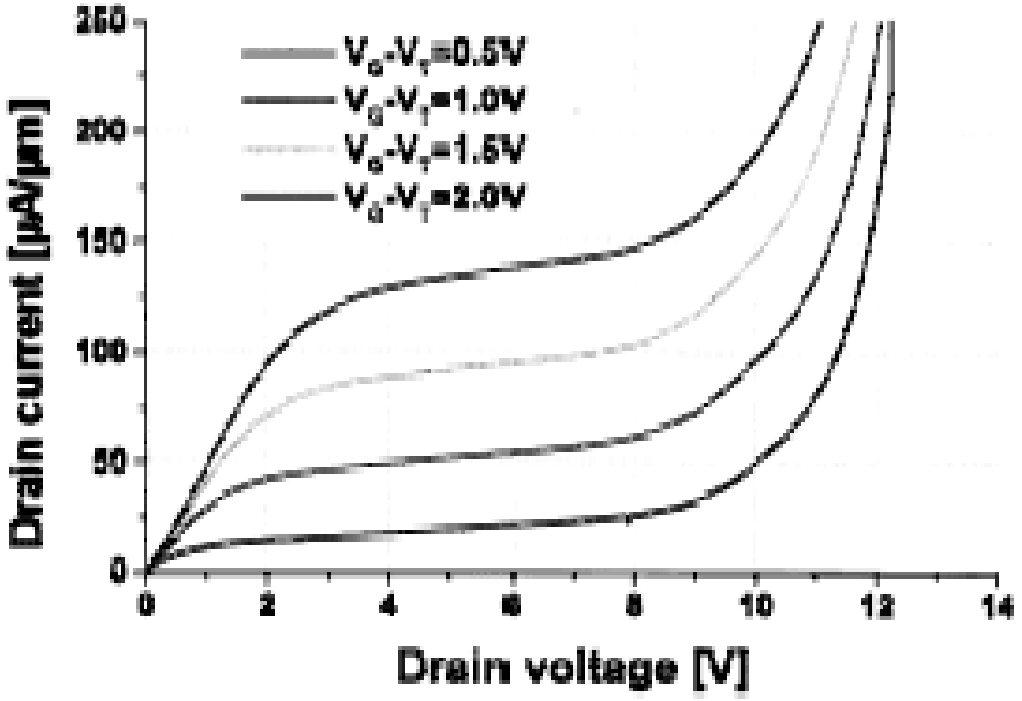
Pre-condition: $\beta_1 \cdot \beta_2 > 1$ & large R_S and R_W

Method for Prevention:

Process: Epi Wafer
high doping/ buried layer
lead to Rs↓, Rw↓
Oxide trench

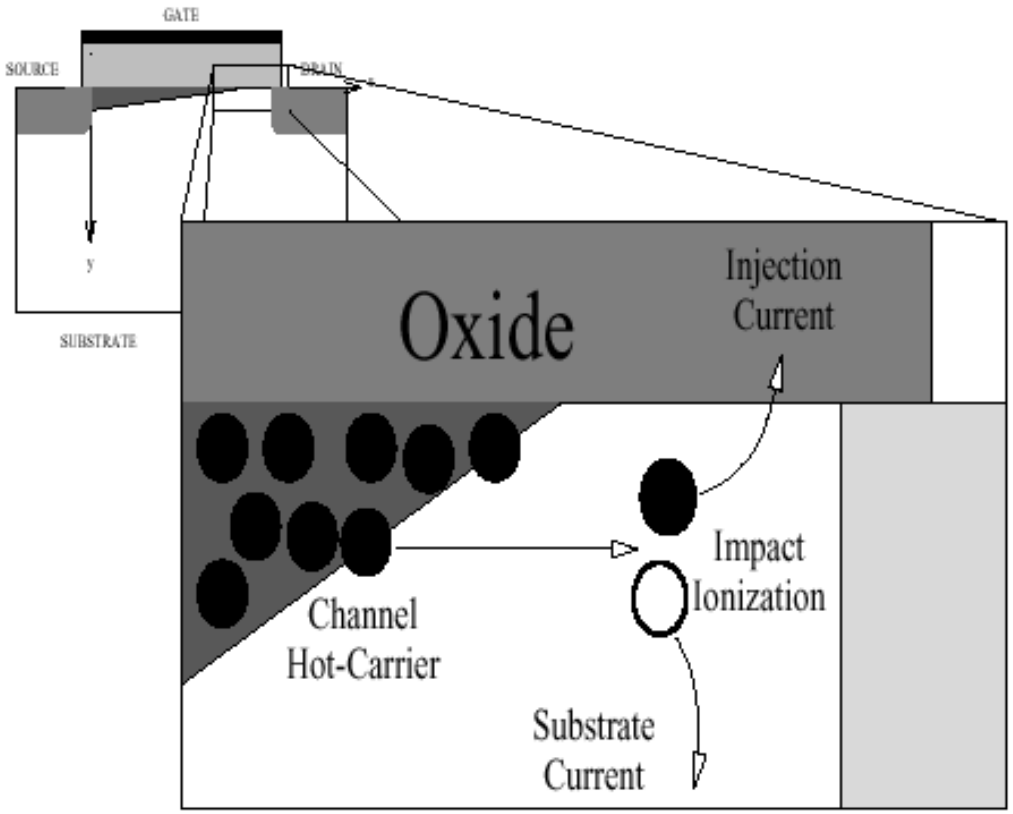
Layout: Large distances lead to small β
Substrate and well contact
lead to Rs↓, Rw↓
guard rings

Break down Effect: Impact Ionization



By drain current (electron or holes) the field strength in the space-charge region will grow.
Thus the impact ionization effect occurs earlier.

Hot Carrier Degradation (1)

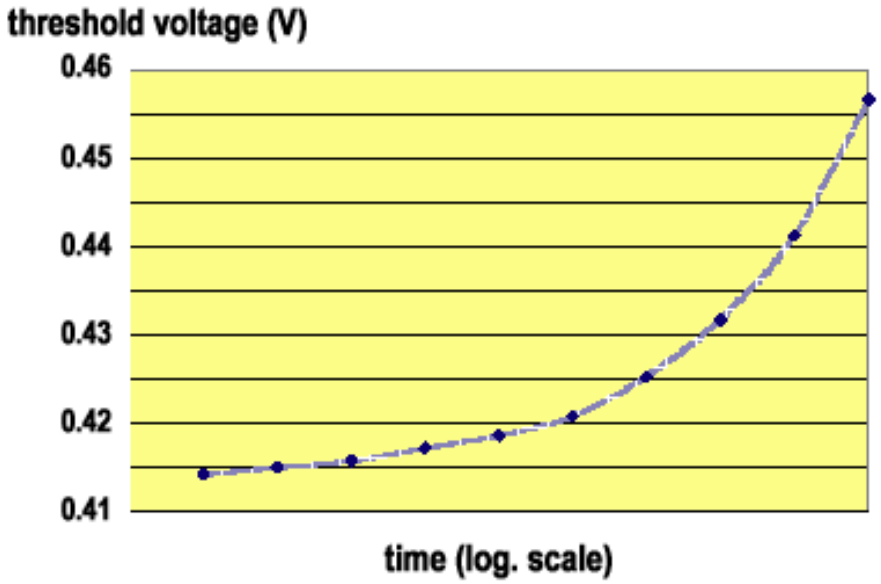


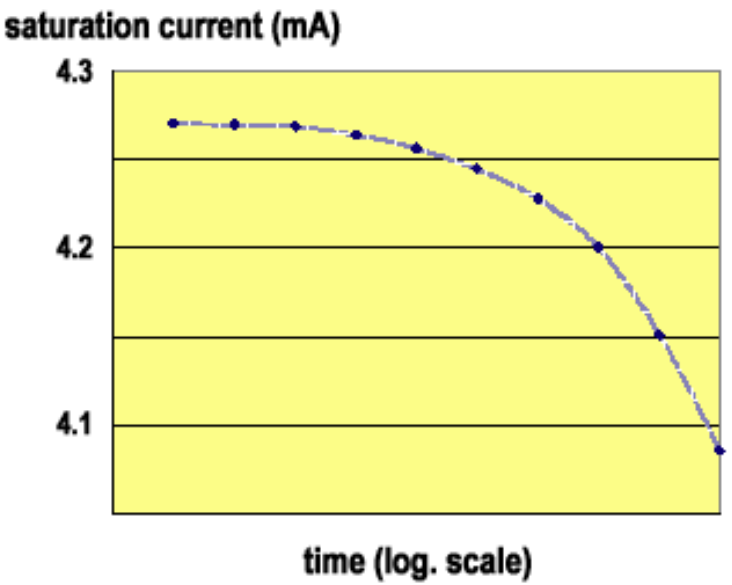
Hot electrons/holes are injected into the thin gate oxide due to high field strength.

Consequence: Shift of threshold voltage and saturation current until to failure (exceeding limits).

Substrate current is a good indicator for impact ionization.

Hot Carrier Degradation (2)





Degradation occurs in time.
Speed depends on Vds, Vgs, Tox and temperature.
(Quick degradation at: high Vds, middle Vgs, thin oxide, low temperature)

NMOS has a three times higher rate of decay (compared to PMOS).

The effect depends also on design.

Process Development
Gate length and Gate oxide

Supply voltage	Technology	Thickness of Gate oxide
5 V	1 μ	20 nm
5 V	0,5 μ	10 nm
3,3 V	0,35μ	6 nm
2,5 V	0,25 μ	5 nm
1,8 V	0,18 μ	3.5 nm