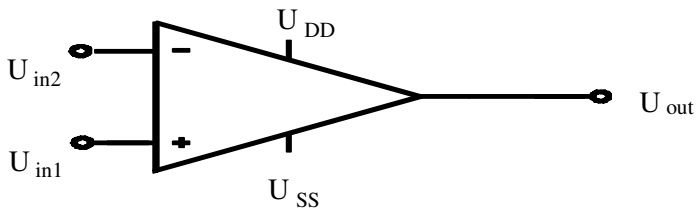
# Chapter 4

## Basis of analog MOS circuit

- Inverter circuit
- Differential amplifier
- Current mirror

# Characteristics of differential amplifier




$$U_{out} = A \cdot (U_{in1} - U_{in2})$$

(The gain A -> infinite)

Uout is saturated high at $U_{DD}$ and low at $U_{SS}$

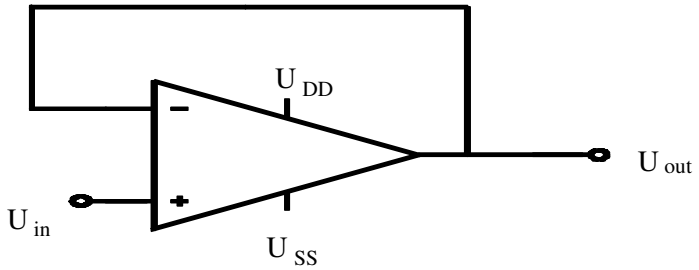
$$I_{in1} = I_{in2} = 0$$

With a proper feedback, $U_{out}$ can ensure that $U_{in1} = U_{in2}$

There is no current in the inputs of the differential amplifier

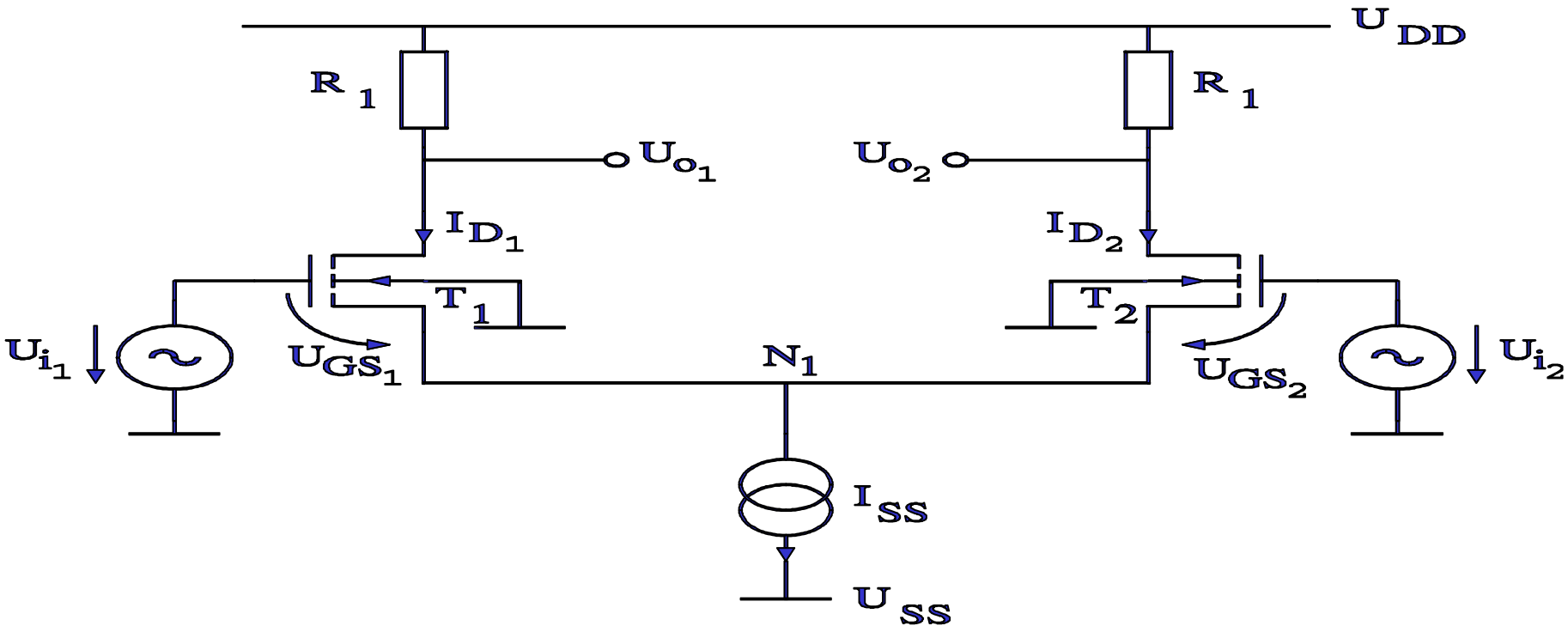
## The buffer circuit

$$A = \frac{U_{out}}{U_{in}} = 1$$




Purpose: $U_{in}$ is unloaded

# Design of differential input




For currents:

$$I_{D1} + I_{D2} = I_{SS}$$

At common mode:

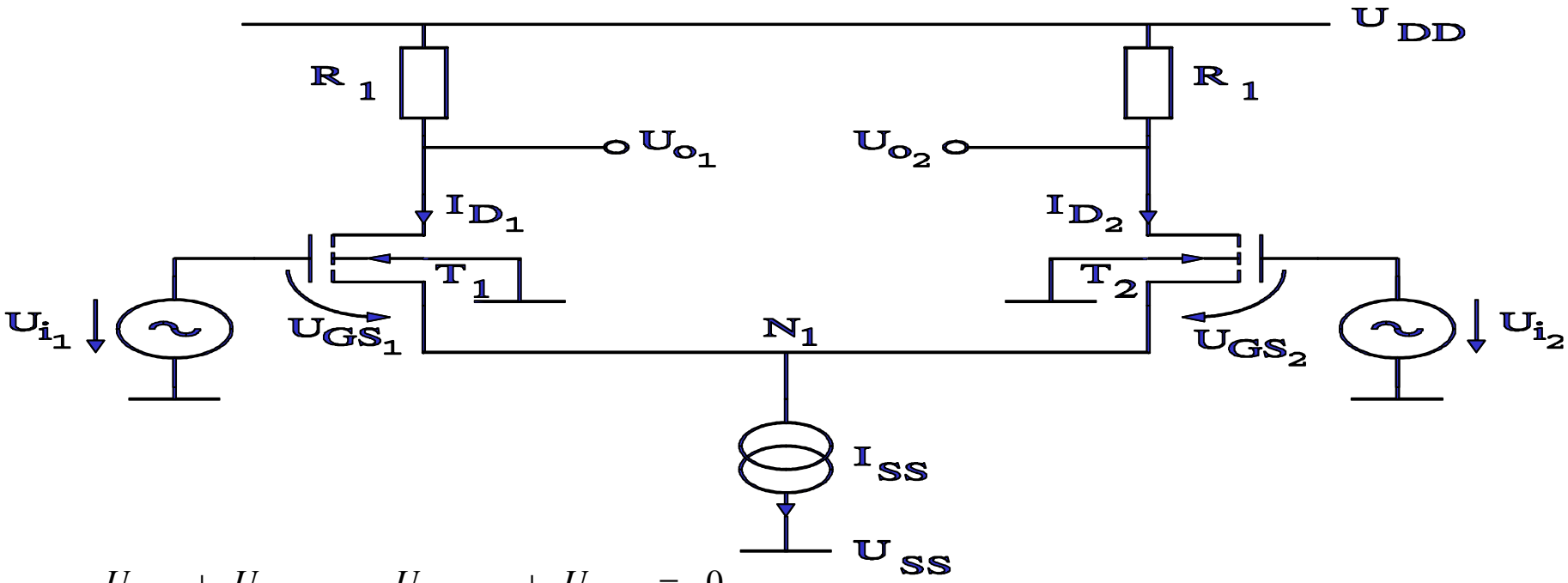
$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

with

$$I_D = \frac{I_{SS}}{2} = \frac{W}{2 \cdot L} \cdot \beta_0 \cdot (U_{GS} - U_T)^2$$

# Operation range (quasi- linear)

## Large signal behaviour




$$-U_{i1} + U_{GS1} - U_{GS2} + U_{i2} = 0$$

$$\underbrace{U_{i1} - U_{i2}}_{\Delta U_i} = U_{GS1} - U_{GS2}$$

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$$I_D = \frac{\beta}{2} \cdot (U_{GS} - U_T)^2 \qquad \Rightarrow \qquad U_{GS} = \sqrt{\frac{2 \cdot I_D}{\beta}} + U_T$$

with $U_{T1} = U_{T2} = U_T$ & $\beta_1 = \beta_2 = \beta$

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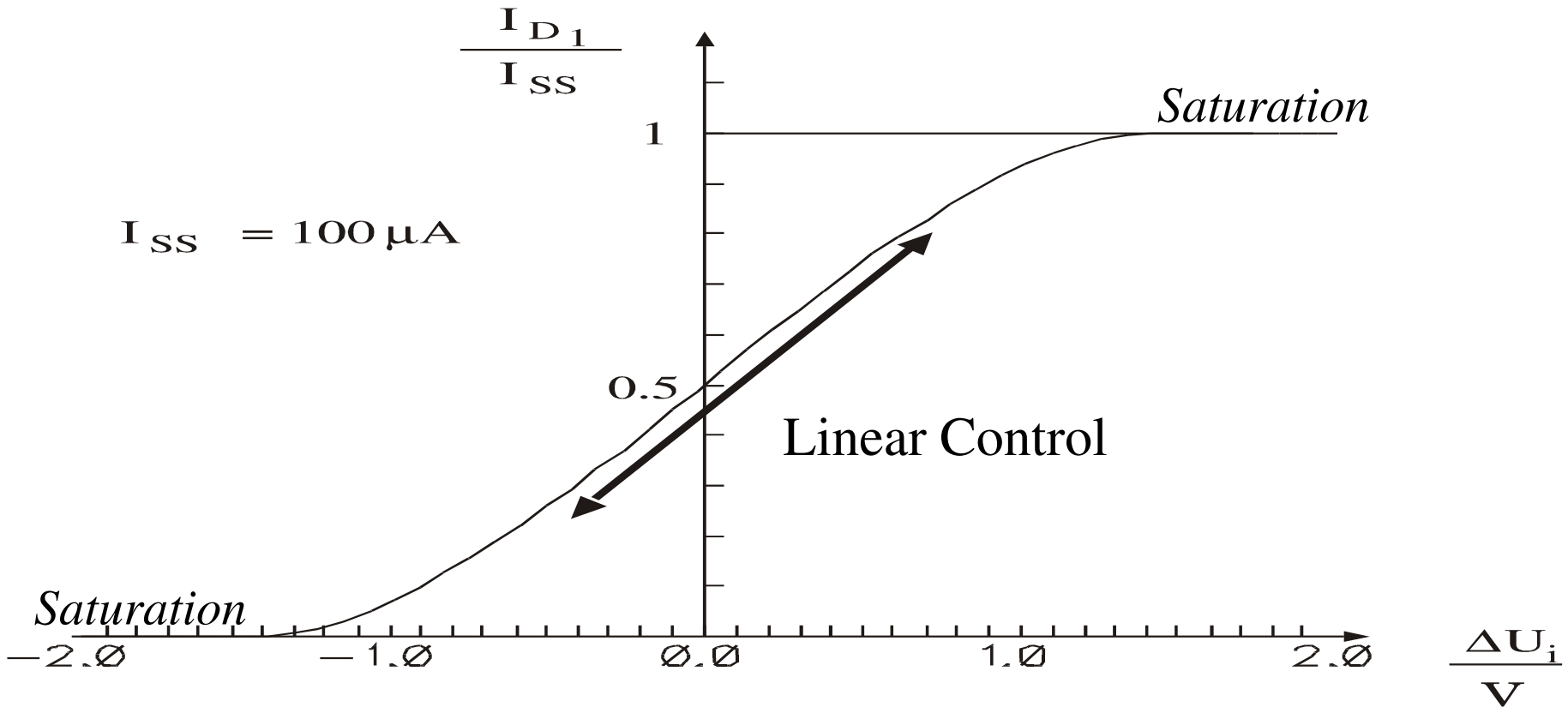
$$\Delta U_i = U_{GS1} - U_{GS2} = \sqrt{\frac{2 \cdot I_{D1}}{\beta}} - \sqrt{\frac{2 \cdot I_{D2}}{\beta}}$$

# Operation range (quasi- linear)
## Large signal behaviour

$$\Delta U_i = U_{GS1} - U_{GS2} = \sqrt{\frac{2 \cdot I_{D1}}{\beta}} - \sqrt{\frac{2 \cdot I_{D2}}{\beta}}$$

mit $I_{D1} + I_{D2} = I_{SS}$ wird $I_{D1} = f(I_{SS}, \Delta U_i)$



# Operation range (quasi- linear)
## Large signal behaviour

***1) Differential voltage***

a) Differential input voltage = 0
(common mode)

$$\Delta U_i = 0 \qquad I_D = \frac{I_{SS}}{2}$$

$$\boxed{U_{GS\,1,2\,o} = \sqrt{\frac{I_{SS}}{\beta}} + U_T}$$

$$\Rightarrow \quad U_{GSeff\;1,2\;o} = \sqrt{\frac{I_{SS}}{\beta}}$$

$$U_{GS} = \sqrt{\frac{2 \cdot I_D}{\beta}} + U_T$$

$$U_{GSeff} = U_{GS} - U_T$$

# Operation range (quasi- linear) Large signal behaviour

***1) Differential voltage***

b) Differential input voltage $< 0$

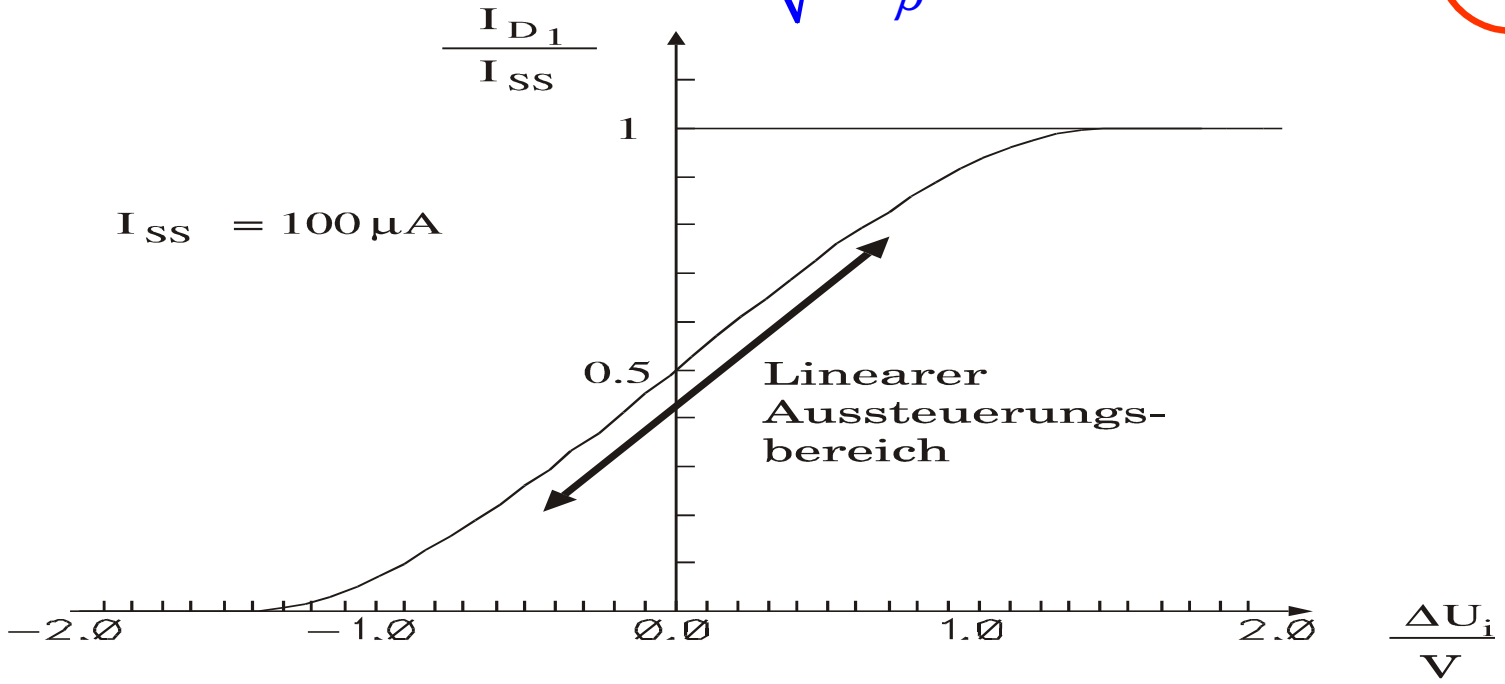
Assumption: $T_1$ is off, 100% of the current $I_{SS}$ through $T_2$

$$U_{GS\,1} \approx U_T \qquad U_{GS\,2} = U_{GSeff\,2} + U_T$$

$$\Delta U_i >> 0 \qquad I_{D\,2} = I_{SS} \qquad U_{GS\,2} = \sqrt{\frac{2 \cdot I_{SS}}{\beta}} + U_T$$

$$\Rightarrow \quad \Delta U_{i\,max} = U_{GS\,2} - U_{GS\,1} = U_{GSeff\,2}$$

$$= \sqrt{\frac{2 \cdot I_{SS}}{\beta}} = \sqrt{2} \cdot U_{GSeff\,1,2\,o}$$



# Operation range (quasi- linear)

## Large signal behaviour

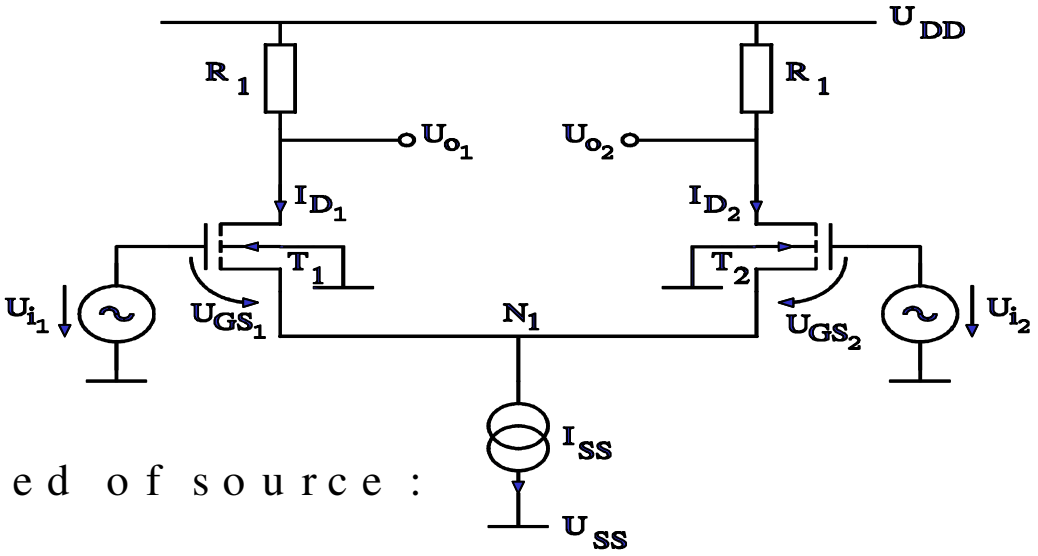
***2) Common Mode Voltage***

a) Maximum common mode input voltage, so that transistors are in saturation

$$U_{DS} \geq U_{GS} - U_{T(U_{SB})}$$

Limit of the saturation:

$$\Rightarrow U_D \overset{!}{=} U_G - U_{T(U_{SB})}$$




Refered to Ground instaed of source:

$U_G = U_{in}$ and $U_D = U_{DD} - I_D \cdot R$

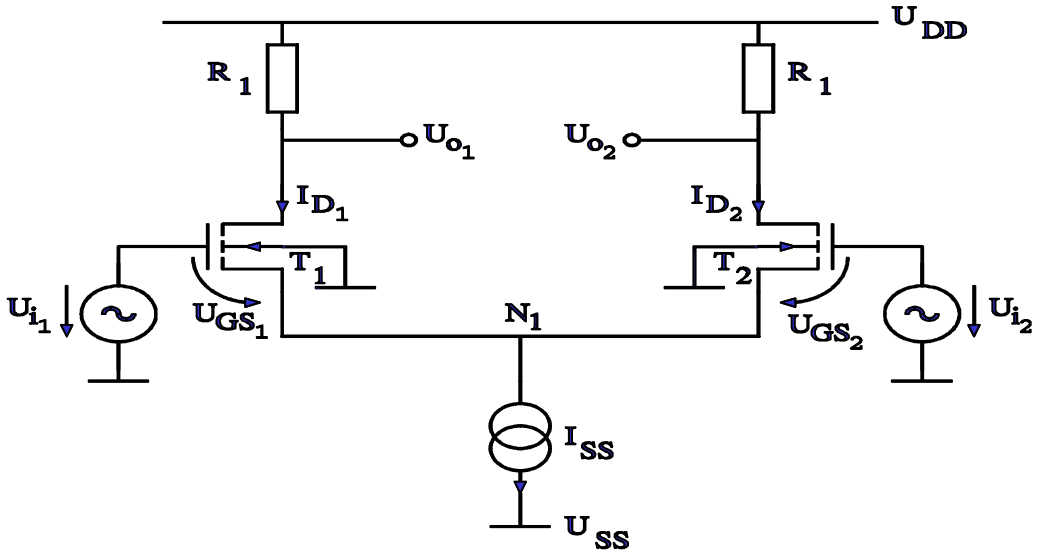
$$\boxed{U_{in\ max} = U_{DD} - \frac{I_{SS}}{2} \cdot R + U_{T(U_{SB}>0)}}$$

$$U_{SB} = U_{N1} = U_{DD} - \frac{I_{SS}}{2} \cdot R - U_{GSeff1,2o}$$

# Operation range (quasi- linear)
## Large signal behaviour

***2) Common Mode***

b) Maximum common mode input voltage, so that transistors are in saturation




Numerical example:

Transistor parameters:

$\beta_0 = 93{,}2\,\mu A/V^2;\ U_T = 1V;\ \gamma = 1\sqrt{V};\ \Phi_D = 0{,}7V$

Circuit parameters:

$I_{SS} = 100\,\mu A;\ R = 10\,k\Omega;\ W/L = 10,\ U_{DD} = 5V$

Calculated operating parameters:

$U_{GSeff1,2o} = 0{,}33V;$

$U_{SB} = 5V - 100\,\mu A \cdot 10\,k\Omega/2 - 0{,}33V = 4{,}17V,\ U_T = 2{,}18V$

maximum constant input voltage:

$U_{in\,max} = 5V - 100\,\mu A \cdot 10\,k\Omega/2 + 2{,}18V = 6{,}68V$

# Operation range (quasi- linear)
## Large signal behaviour

***2) Common Mode***

b) minimum common mode input voltage, so that current $I_{SS}$ can flow

$$U_{GS_{1,2}} = \sqrt{\frac{I_{SS}}{\beta}} + U_{T(U_{SB})}$$

Node potential $U_{N1}$ minimum $U_{SS}$ -> $U_{SB}=0$

$$U_{in\,min} = \sqrt{\frac{I_{SS}}{\beta}} + U_T + U_{SS} \qquad \text{mit} \qquad U_{SB} \approx 0$$

## Numerical example:

Transistor parameters:

$\beta_0 = 93{,}2\,\mu A/V^2;\ U_T = 1V;\ \gamma = 1\sqrt{V};\ \Phi_D = 0{,}7V$

Circuit parameters:

$I_{SS} = 100\,\mu A;\ R = 10\,k\Omega;\ W/L = 10,\ U_{DD} = 5V$

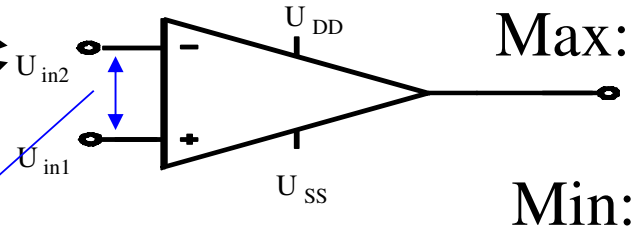
$U_{in\,min} = 1{,}33V$ abobe $U_{SS}$

$U_{in\,max} - U_{in\,min} = 6{,}68V - 1{,}33V = 5{,}55V \approx U_{DD} - U_{SS}$

# Operation range (quasi- linear)

## Common Mode Input

$$U_{in\,max} = U_{DD} - \frac{I_{SS}}{2} \cdot R + U_T \quad (U_{SB} > 0)$$




output

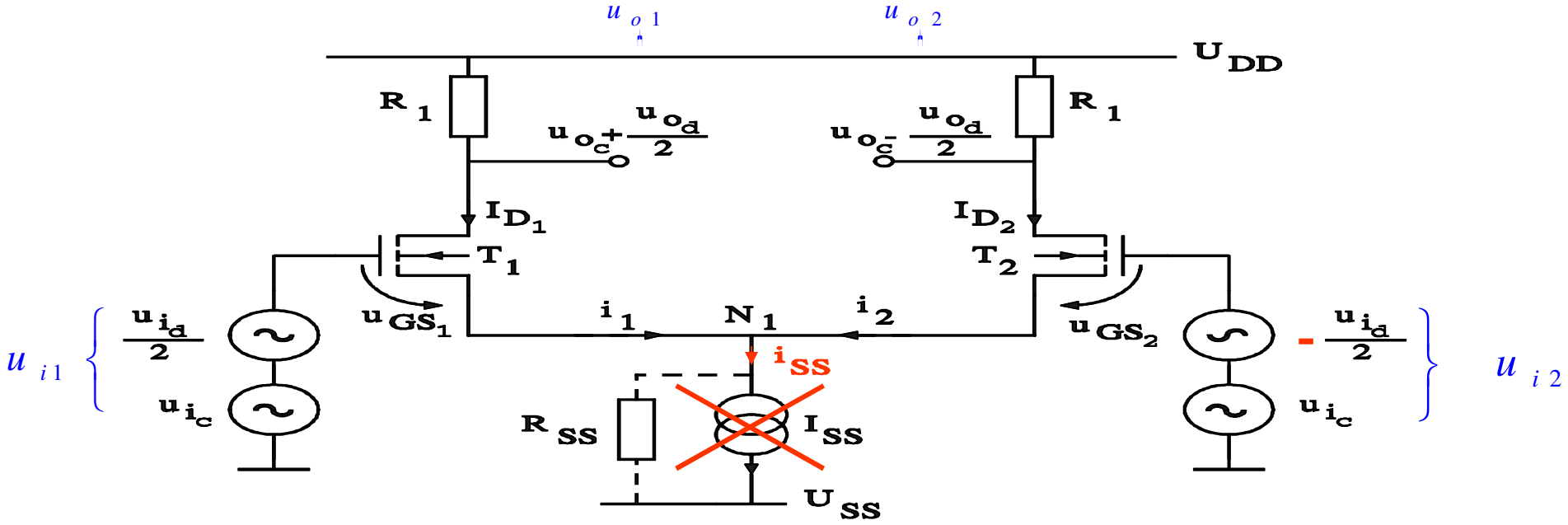
Max: $U_{DD}$

Min: $U_{SS}$

$$U_{in\,min} = \sqrt{\frac{I_{SS}}{\beta}} + U_T$$

Maximum input difference: $\sqrt{\frac{2 \cdot I_{SS}}{\beta}}$

# Small signal behaviour




Splitting into common mode and differential voltage

$$u_{id} = u_{i1} - u_{i2} \qquad u_{od} = u_{o1} - u_{o2}$$

$$u_{ic} = \frac{u_{i1} + u_{i2}}{2} \qquad u_{oc} = \frac{u_{o1} + u_{o2}}{2}$$

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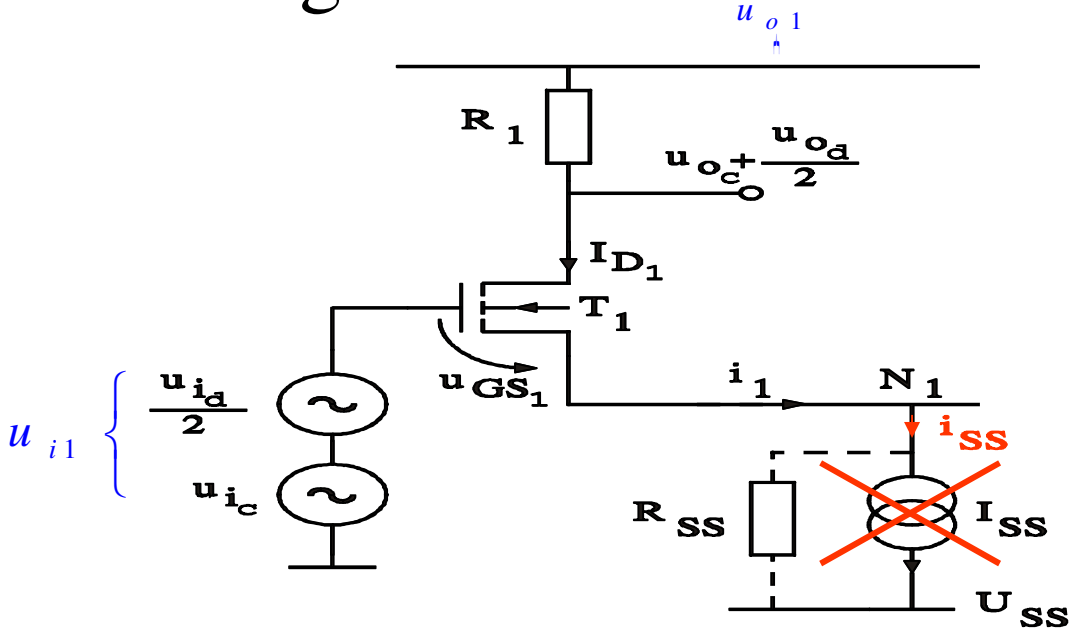
$$u_{i1} = u_{ic} + \frac{1}{2} \cdot u_{id} \qquad u_{o1} = u_{oc} + \frac{1}{2} \cdot u_{od}$$

$$u_{i2} = u_{ic} - \frac{1}{2} \cdot u_{id} \qquad u_{o2} = u_{oc} - \frac{1}{2} \cdot u_{od}$$

# Small signal behaviour




## Differential Mode

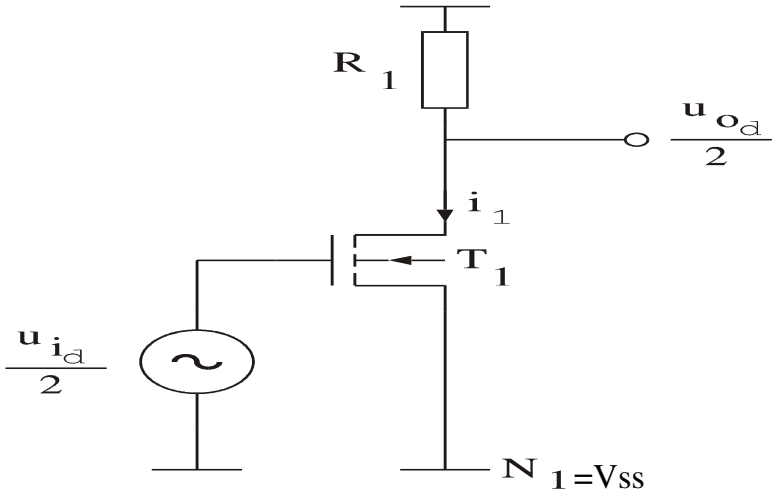
$$u_{i1} = u_{ic} + \frac{1}{2}\cdot u_{id} \qquad u_{i2} = u_{ic} - \frac{1}{2}\cdot u_{id}$$

$$u_{ic} = 0 \quad \Rightarrow \quad u_{oc} = 0$$

$$\frac{1}{2}\cdot u_{id} = \left|-\frac{1}{2}\cdot u_{id}\right| \quad \Rightarrow \quad i_1 = -i_2 \quad \Rightarrow \quad i_{ss} = 0$$

=> N1 is in small signal domian behaviour ground!

# Equivalent circuit diagram for differential mode (Small signal behaviour)

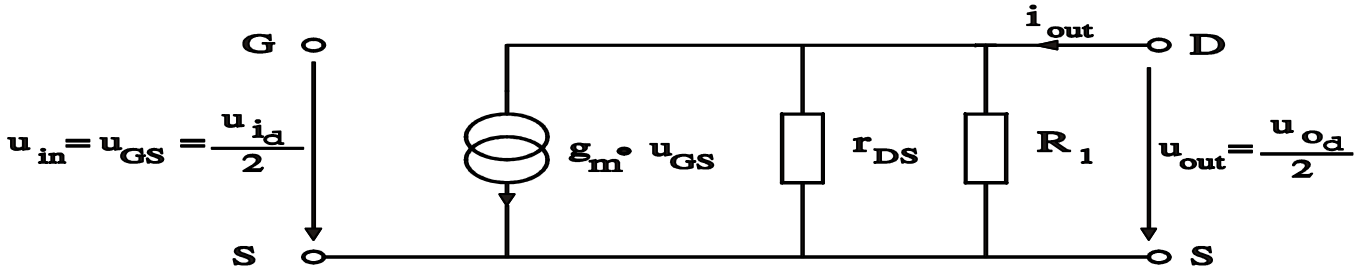



$$\frac{1}{2} \cdot u_{od} = A_{VDM} \cdot \frac{1}{2} \cdot u_{id}$$

$$A_{VDM} = -g \cdot r_{out}$$

$$= -g_{m1} \cdot (R_1 \| r_{DS1})$$

$$\approx -g_{m1} \cdot R_1$$

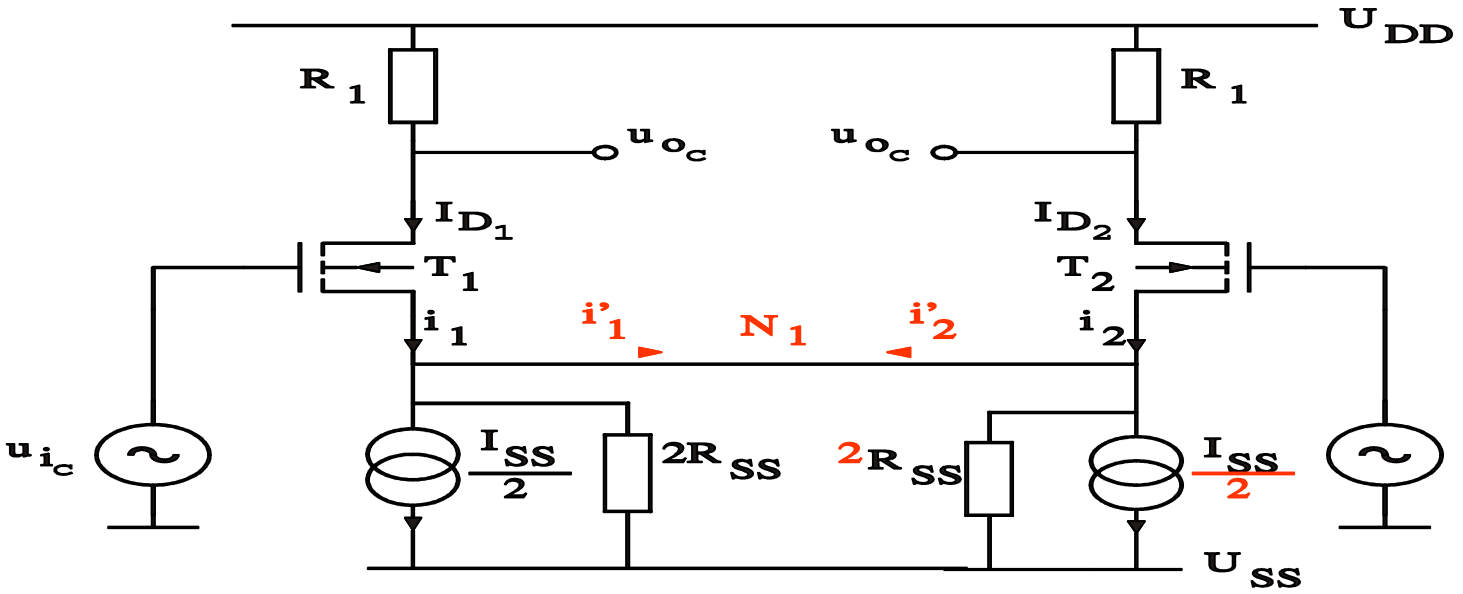



$$g = \left.\frac{i_{out}}{u_{in}}\right|_{u_{out}=0} = \frac{g_m \cdot \frac{1}{2} \cdot u_{id}}{\frac{1}{2} \cdot u_{id}} = g_m$$

$$r_{out} = \left.\frac{u_{out}}{i_{out}}\right|_{u_{in}=0} = r_{DS1} \| R_1 = \frac{1}{\frac{1}{R_1} + \frac{1}{r_{DS1}}}$$

# Equivalent circuit diagram for common mode

## (Small signal behaviour)




$$u_{id} = 0$$

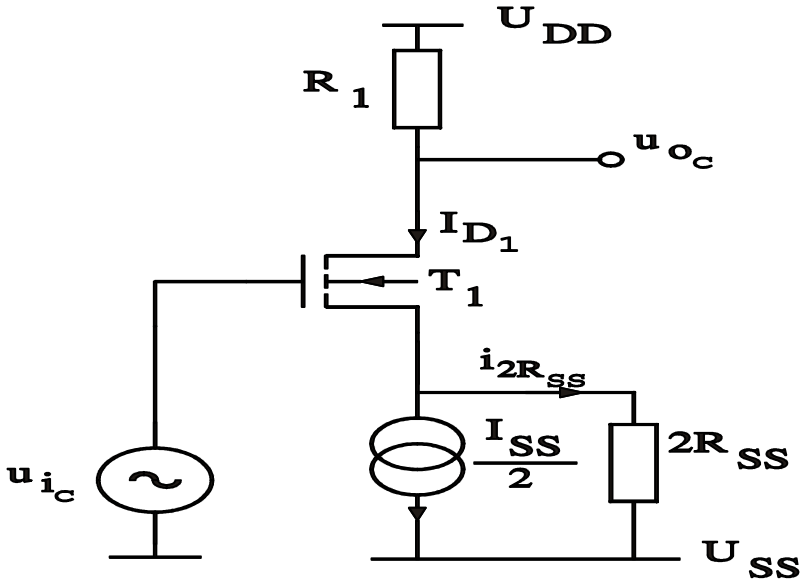
$$\Rightarrow u_{od} = 0$$

$$u_{ic} = u_{ic}$$

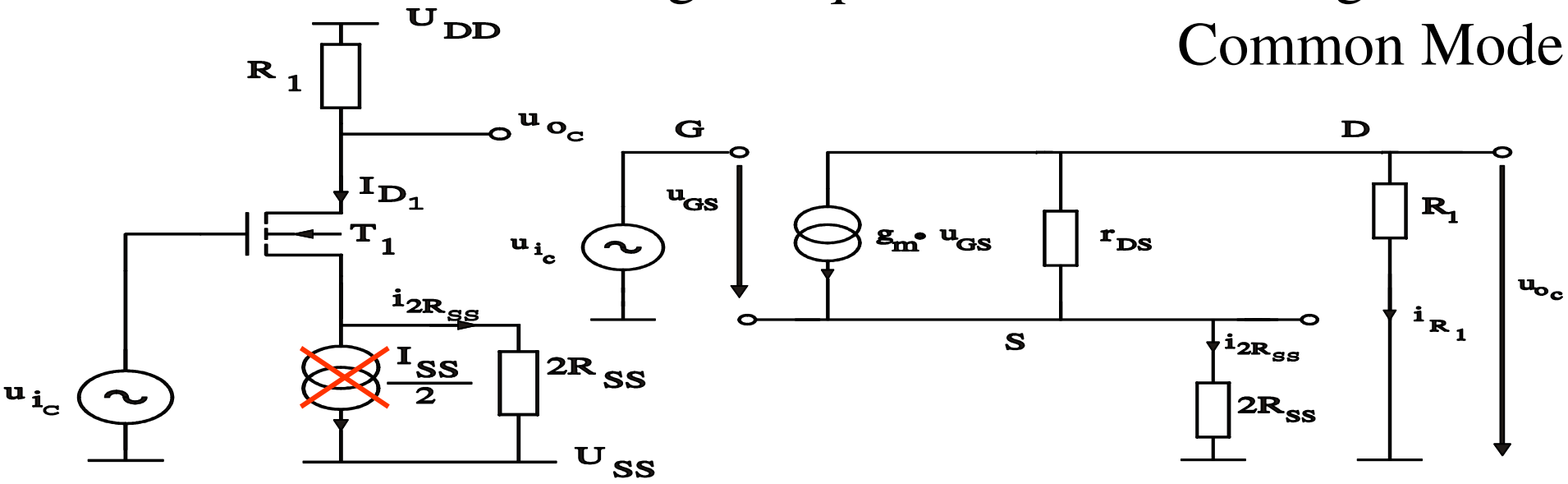
$$\Rightarrow i_1 = i_2$$

$$\Rightarrow i_1' = i_2' = 0$$

⇒No current flows via N1!



# Small signal equivalent ciurcuit diagram for Common Mode




$$u_{ic} = u_{GS} + i_{2RSS} \cdot 2 \cdot R_{SS}$$

$$u_{oc} = -i_{2RSS} \cdot R_1$$

$$u_{oc} = i_{2RSS} \cdot 2 \cdot R_{SS} + (i_{2RSS} - g_m \cdot u_{GS}) \cdot r_{DS}$$

$$\left.\frac{i_{out}}{u_{out}}\right|_{u_{ic}=0} = ? \quad \Rightarrow \quad r_{out}$$

$$\left.\frac{i_{out}}{u_{in}}\right|_{u_{oc}=0} = ? \quad \Rightarrow \quad g$$

$$A_{VCM} = \frac{U_{OC}}{U_{IC}} = \frac{-g_m}{\cancel{\frac{1}{r_{DS}}} + \frac{1}{R_1} + \frac{2 \cdot R_{SS}}{R_1} \cdot \left(\cancel{\frac{1}{r_{DS}}} + g_m\right)} = \frac{-g_m}{\frac{1}{R_1} \cdot \left(\cancel{1} + 2 \cdot R_{SS} g_m\right)}$$

mit $r_{DS} >> R_1$, $g_m >> g_{DS} = \frac{1}{r_{DS}}$ und $2 \cdot R_{SS} \cdot g_m >> 1$

$$A_{VCM} \approx -\frac{R_1}{2 \cdot R_{SS}}$$

# Common Mode Rejection Ratio: CMRR

$$A_{VDM} \approx -g_{m1} \cdot R_1$$

$$A_{VCM} \approx -\frac{R_1}{2 \cdot R_{SS}}$$

$$CMRR = \frac{A_{VDM}}{A_{VCM}} = 2 \cdot g_{m1} \cdot R_{SS}$$

For a good differential amplifier:

- R1 uncritical
- high Gm
- high Rss

# By now:

$$A_{INV} \approx A_{VDM} \approx -g_{m1} \cdot R_1$$

$$CMRR = \frac{A_{VDM}}{A_{VCM}} = 2 \cdot g_{m1} \cdot R_{SS}$$

What next?

How to realize a high $g_m$ ?

$$g_m = \frac{dI_D}{dU_{GS}} \qquad I_D = \frac{\beta}{2} \cdot (U_{GS} - U_T)^2$$

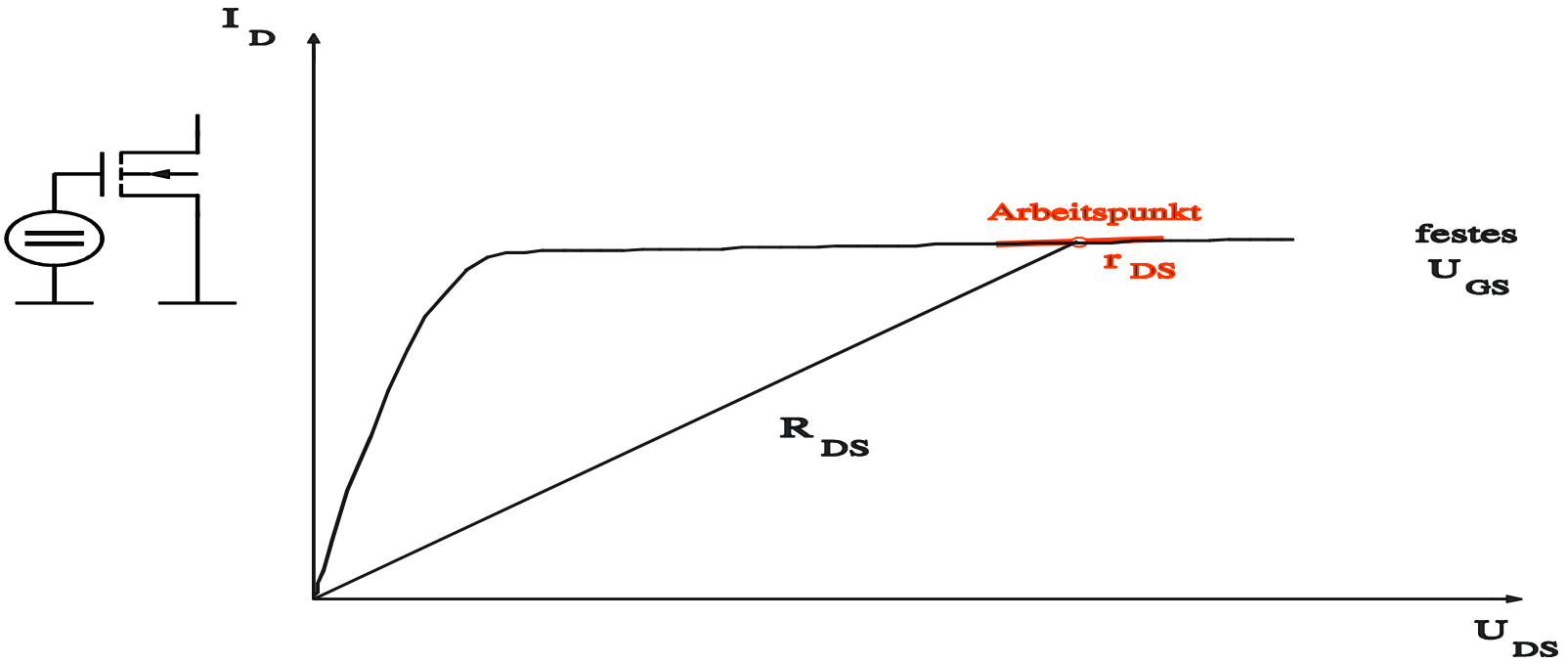
$$g_m = \beta \cdot (U_{GS} - U_T)$$

$$= \beta \cdot U_{GSeff} \qquad = \sqrt{2 \cdot I_D \cdot \beta} \qquad = \frac{2 \cdot I_D}{U_{GSeff}}$$

and

How to realize high resistances $R_{SS}$?

# Transistors as resistor




$$\frac{dI_D}{dU_{DS}} = g_{DS} = \frac{1}{r_{DS}}$$

Small signal resistance

$$G = 1/R = \frac{I_D}{U_{DS}}$$

Large signal resistance

$$g_{DS} = I_D \cdot \lambda \quad \Rightarrow \quad g_{DS} = 9,3\ \mu S$$

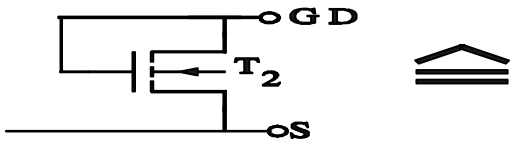
$$r_{DS} = 110\ k\Omega$$

$$\Rightarrow \quad R_{DS} = 20\ k\Omega$$

Fixed potential ($U_{GS}$) necessary: other solution?

# 1) Transistor in „Diode circuit“

*a) n-channel transistor*





$$U_{DS} = U_{GS}$$

$$\Rightarrow U_{DS} > U_{GS} - U_T$$

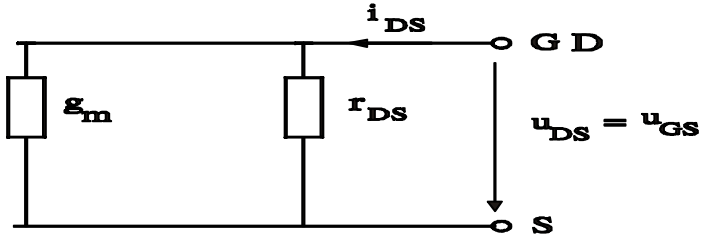
$$\Rightarrow \text{Sättigung}$$

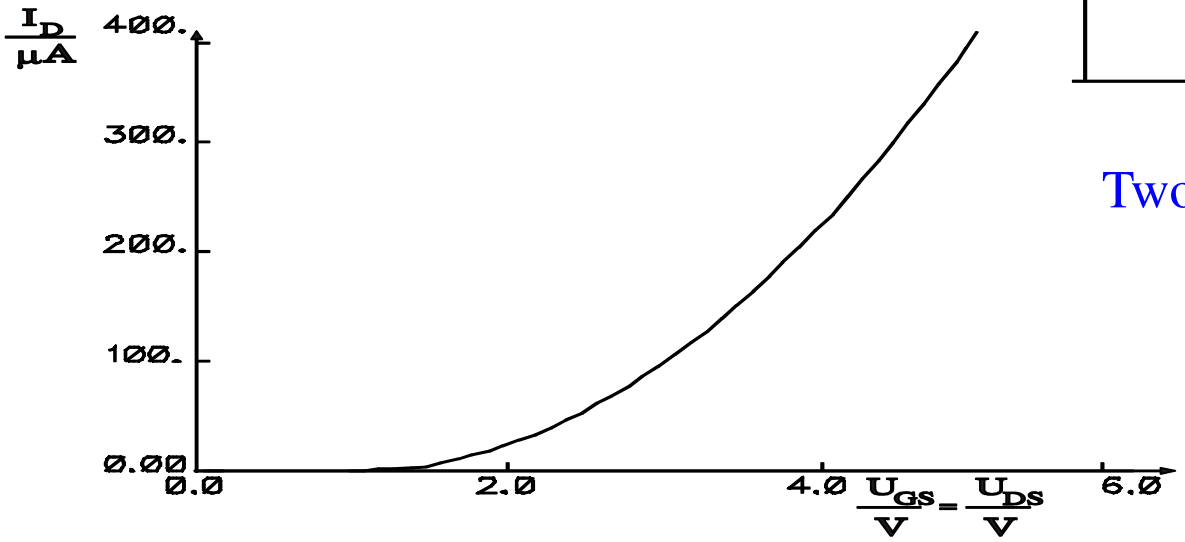
$$\Rightarrow I_D = \frac{\beta}{2}(U_{GS} - U_T)^2$$

$$r_{out} = \frac{u_{out}}{i_{out}} = \frac{u_{DS}}{i_{out}}$$

$$i_{out} = g_m \cdot u_{DS} + g_{DS} \cdot u_{DS}$$

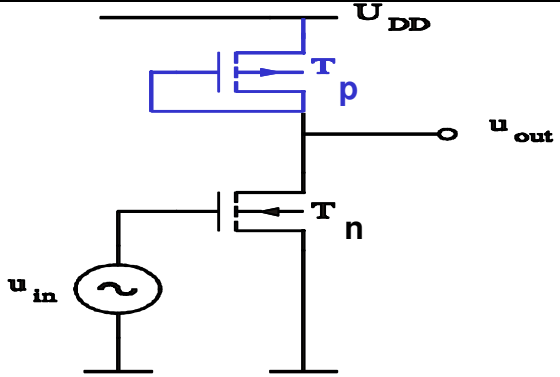
$$r_{out} = \frac{1}{g_m + g_{DS}} \approx \frac{1}{g_m} \quad (\approx 1\,k\,\Omega)$$

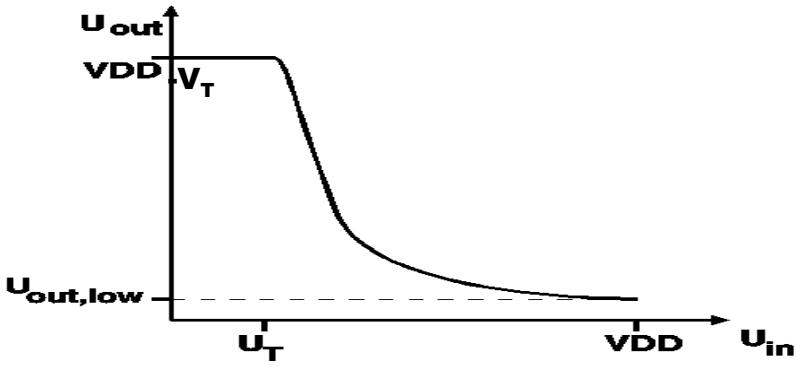


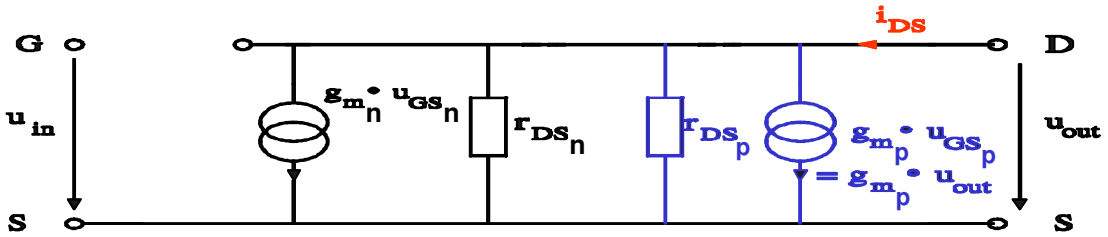




Two-terminal-device „*Diode*“

## *b) p-channel transistor as the load of an inverter*




$$A_V = -g_m \cdot r_{out}$$

with $g_m = g_{mn}$ und

$$r_{out} = \frac{1}{g_{mp} + g_{DSn} + g_{DSp}} \approx \frac{1}{g_{mp}}$$

$$A_V = -\frac{g_{mn}}{g_{mp}}$$

$$g_{mp} = \sqrt{2 \cdot I_D \cdot \beta_{0P} \cdot \left(\frac{W}{L}\right)_p} \qquad g_{mn} = \sqrt{2 \cdot I_D \cdot \beta_{0n} \cdot \left(\frac{W}{L}\right)_n}$$

$$A_V = -\sqrt{\frac{\beta_{0n} \cdot \left(\frac{W}{L}\right)_n}{\beta_{0p} \cdot \left(\frac{W}{L}\right)_p}} \approx -\sqrt{\frac{3 \cdot \left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p}}$$

Example:

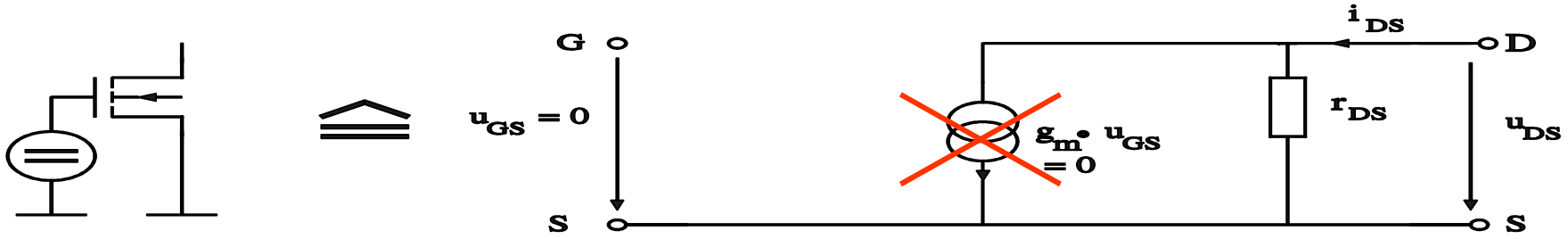
$$A_V = -\sqrt{\frac{\beta_{0n} \cdot \left(\frac{W}{L}\right)_n}{\beta_{0p} \cdot \left(\frac{W}{L}\right)_p}} \approx -\sqrt{\frac{3 \cdot \left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p}}$$

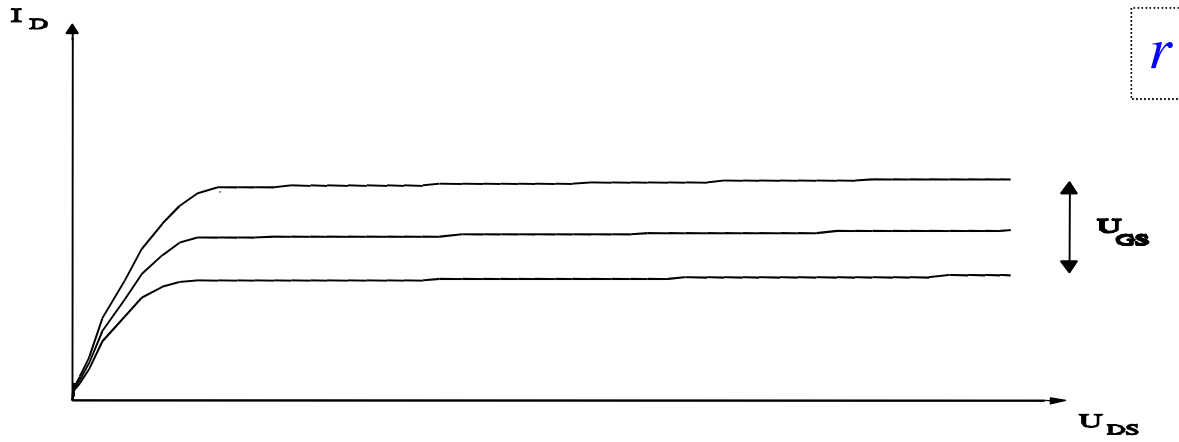
$$A_V = -\sqrt{\frac{3 \cdot \left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p}} = -\sqrt{\frac{3 \cdot \left(\frac{50}{5}\right)_n}{\left(\frac{5}{15}\right)_p}} \approx -10$$

Summary: MOS-diode provides only small resistance,
as transconductance Gm contributes to the conductance.
⇨ long channel length is necessary

# 2) Transistor with fixed gate potential

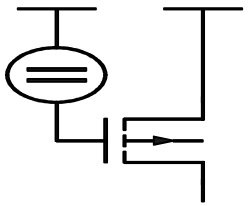
*a) n-channel transistor with $U_G$=const.*



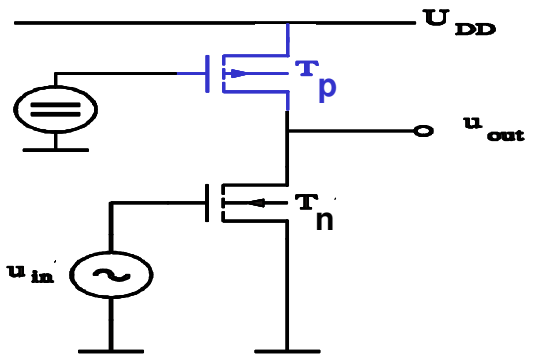



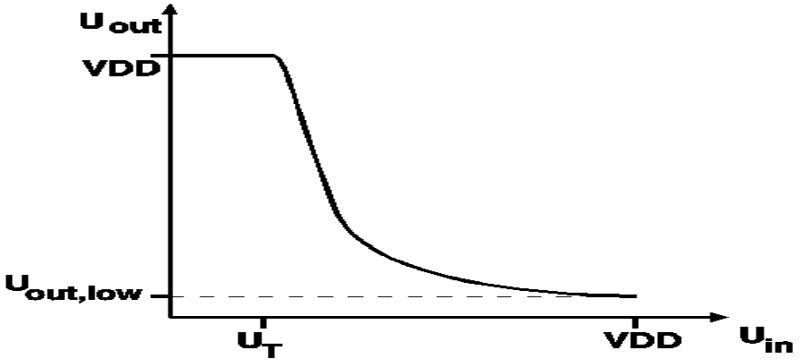

$$r_{out} = r_{DS}$$

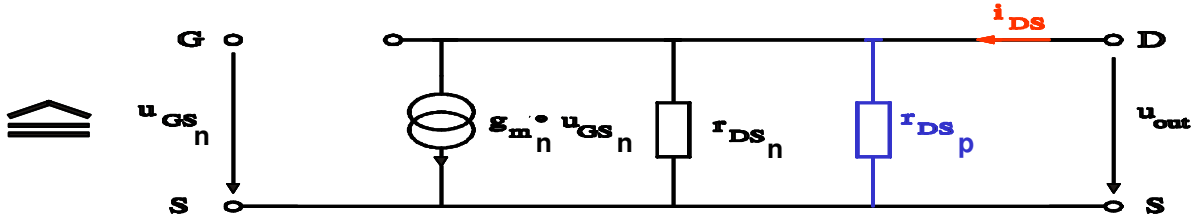
*b) p-channel transistor with $U_G$=const.*



## *b) Transistor with $U_G$=const. as load of an inverter*




$$A_V = -g_m \cdot r_{out}$$

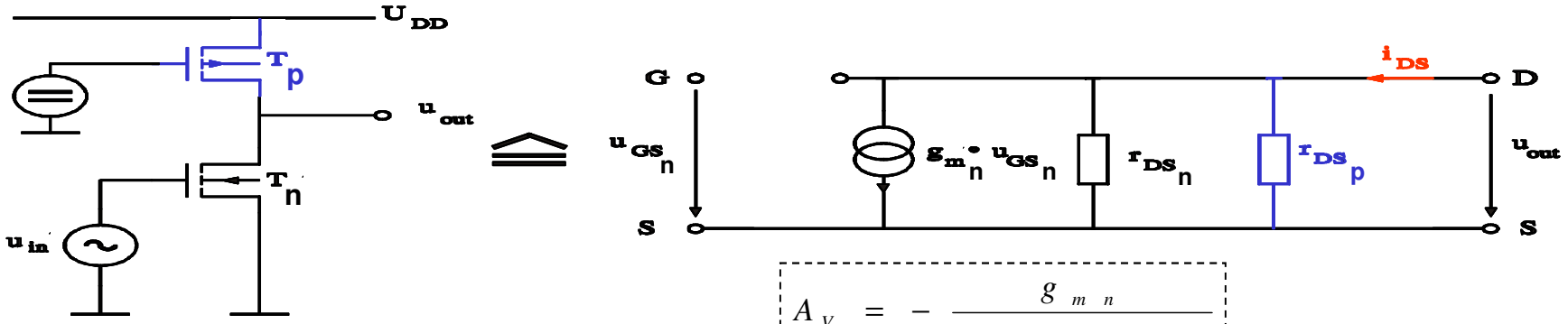
with $g_m = g_{mn}$ and $r_{out} = r_{DSn} \parallel r_{DSp} = \dfrac{1}{g_{DSn} + g_{DSp}}$

$$A_V = -\frac{g_{mn}}{g_{DSn} + g_{DSp}}$$

Example:

$$A_V = -\frac{500\ \mu S}{2.5\ \mu S + 2.5\ \mu S} \approx -100$$

# Transistor with $U_G$=const. as load




$$A_V = -\frac{g_{m\,n}}{g_{DSn} + g_{DSp}}$$

n-channel is driven /
p-channel as load

$$A_V = -\frac{g_{m\,p}}{g_{DSn} + g_{DSp}}$$

p-channel is driven /
n-channel as load