Up to Now:

Devices are transistors (diodes), resistances etc.

You can make analog circuits like
inverter, amplifier or current source

And the next?

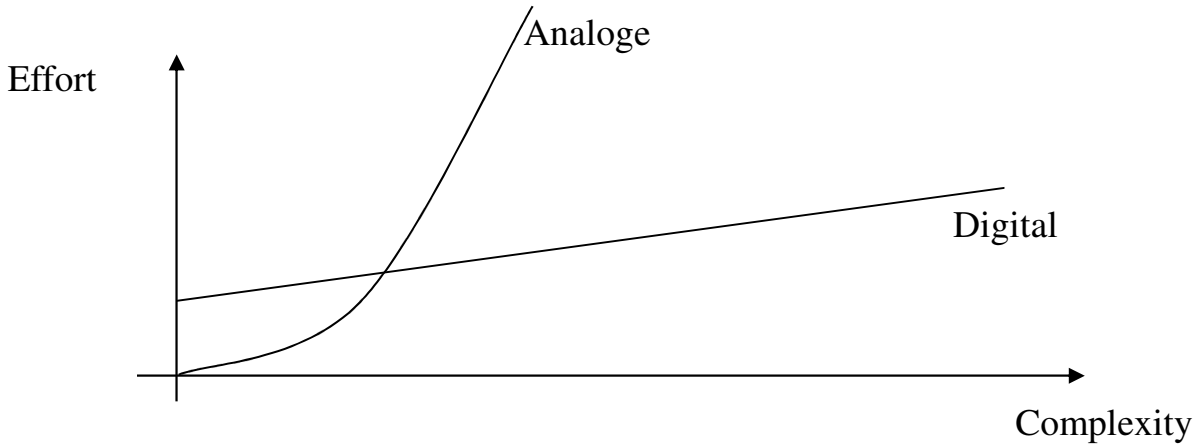
How to design **digital circuits**
with these devices / transistors?

Chapter 4 Contents

- Introduction of digital circuitry
- Digital MOS-circuits
- CMOS - complementary MOS
- Pseudo-NMOS (p-channel-transistor as load)
- Delays
- Power Consumption

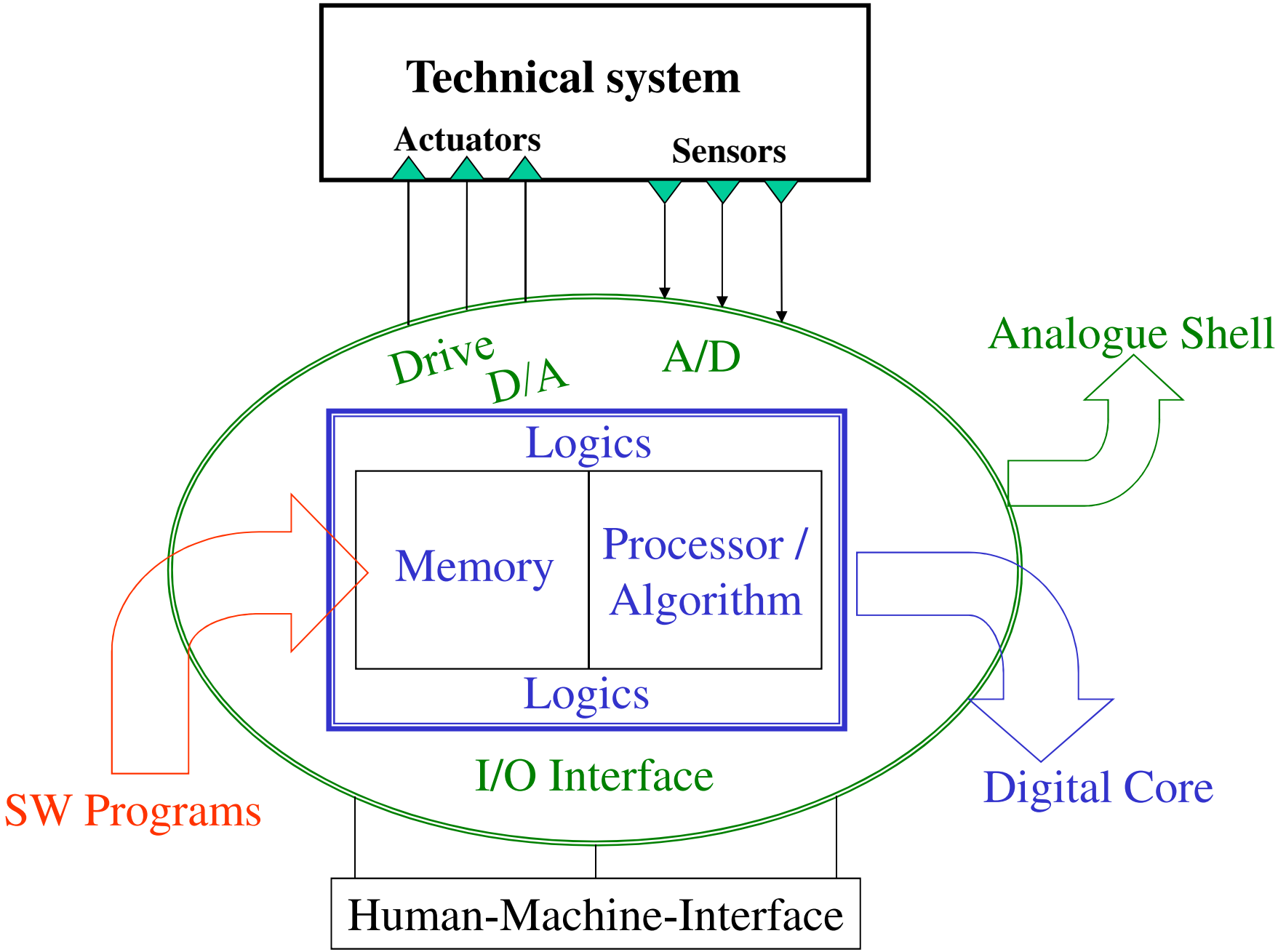
Advantages of digital circuit technology

- Possibility of simple and error-free processing, so that great complexity can be mastered.
- Tolerant to variation in production

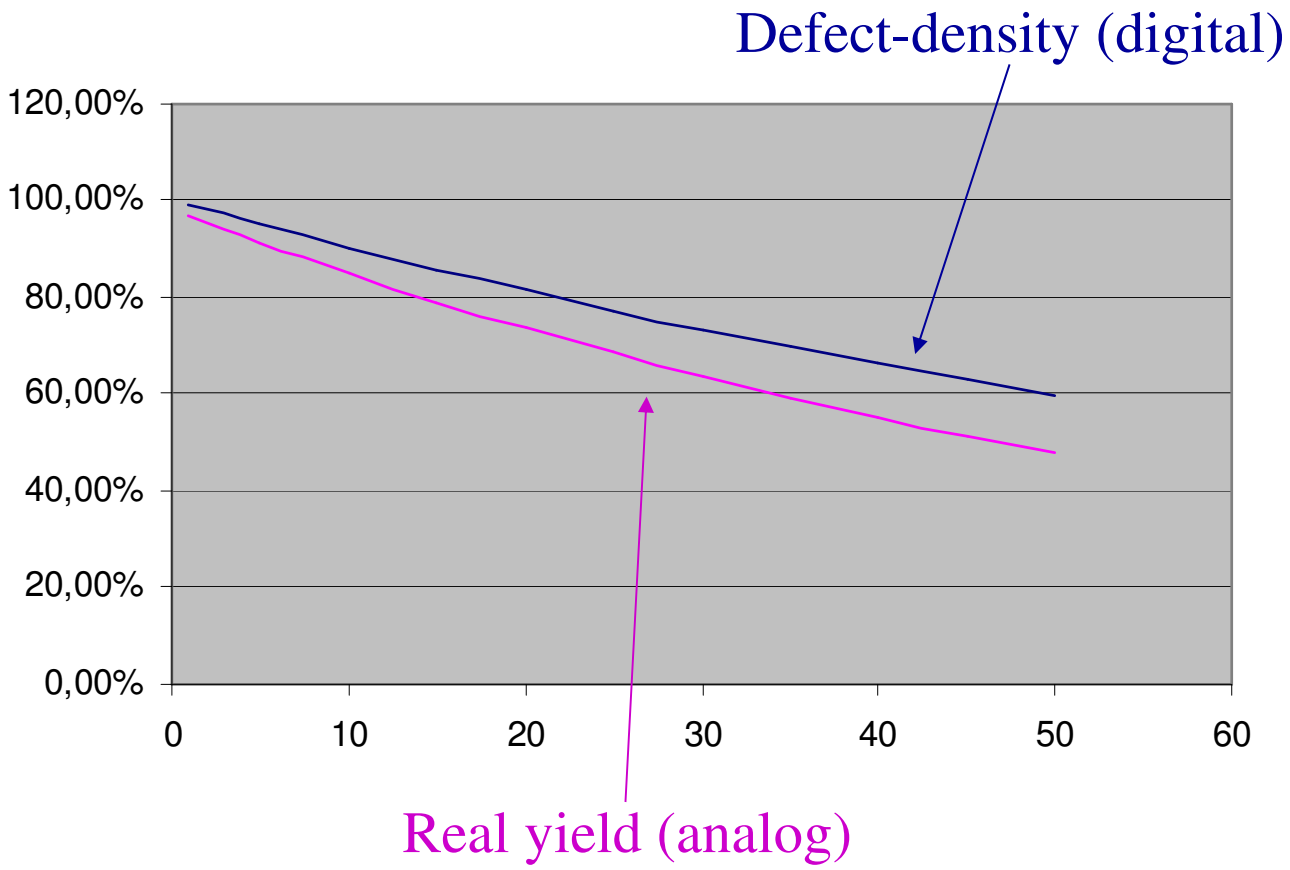


- Digital means discrete values (binary) and discrete time!
- High resolution is achieved by more bits (parallel) and clocks (sequential).

Necessary: clock generator, A/D- and D/A-converter


Technical system
Actuators
Sensors
Drive
D/A
A/D
Analogue Shell
Logics
Memory
Processor /
Algorithm
Logics
I/O Interface
SW Programs
Digital Core
Human-Machine-Interface

Yield Dependence on Chip Size

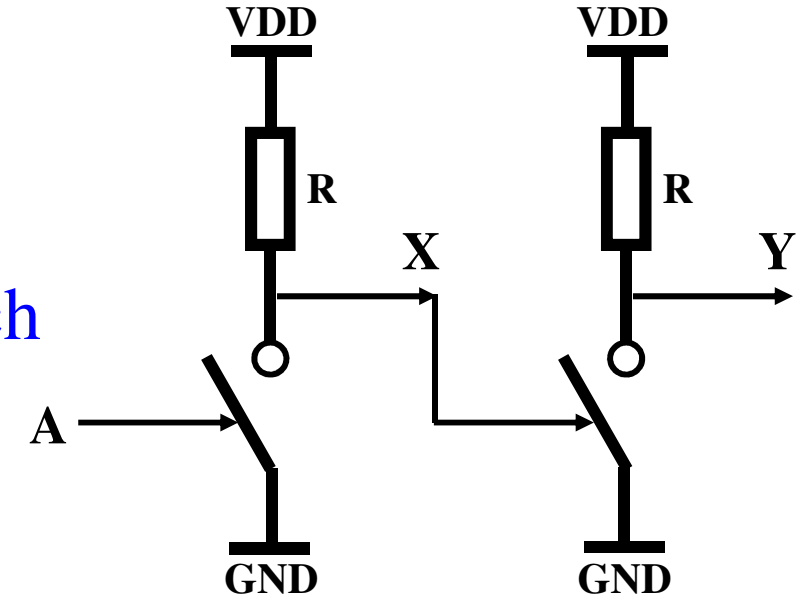


The yield of digital circuits does not depend on design.
Precondition: process, models and library are alright

Switch Network

Digital circuit (bipolar, MOS)

Transistor as a switch



A	State	X		Y
0	Switch on	1	Switch off	0
1	Switch off	0	Switch on	1

BUT

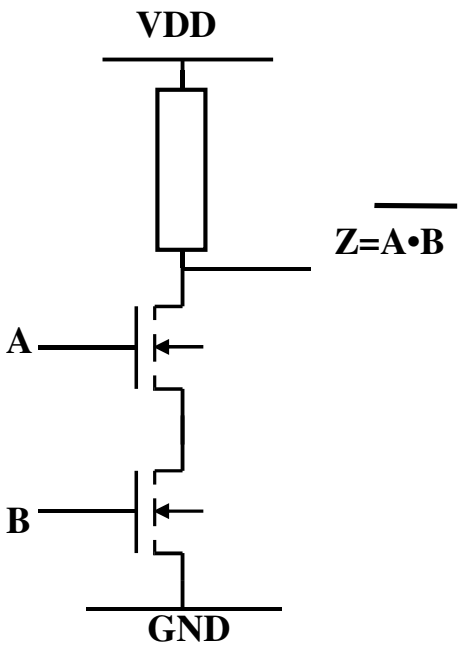
These switches are transistors and have a threshold voltage.

These switches have a on-resistance.

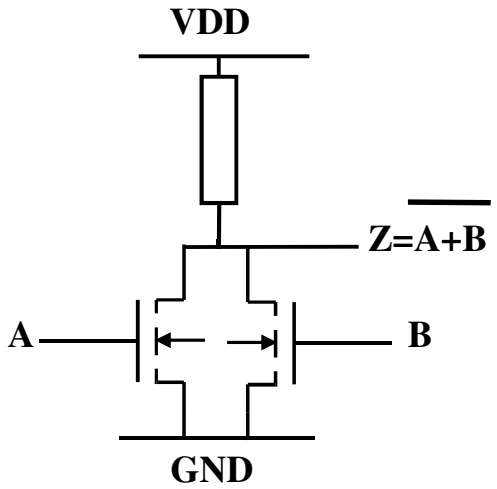
Switch on: $U_{in}>U_T$; Switch off: $U_{in}<U_T$

Switch on: Voltage divider U_{out}=?

Realization of Gates



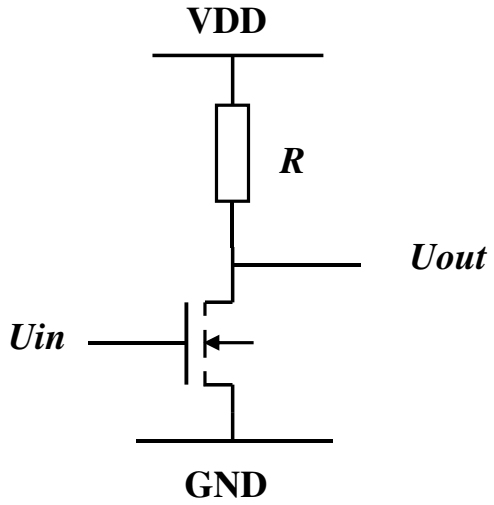
NAND-Gate



NOR-Gate

Gate is the lowest abstraction level of digital circuitry.

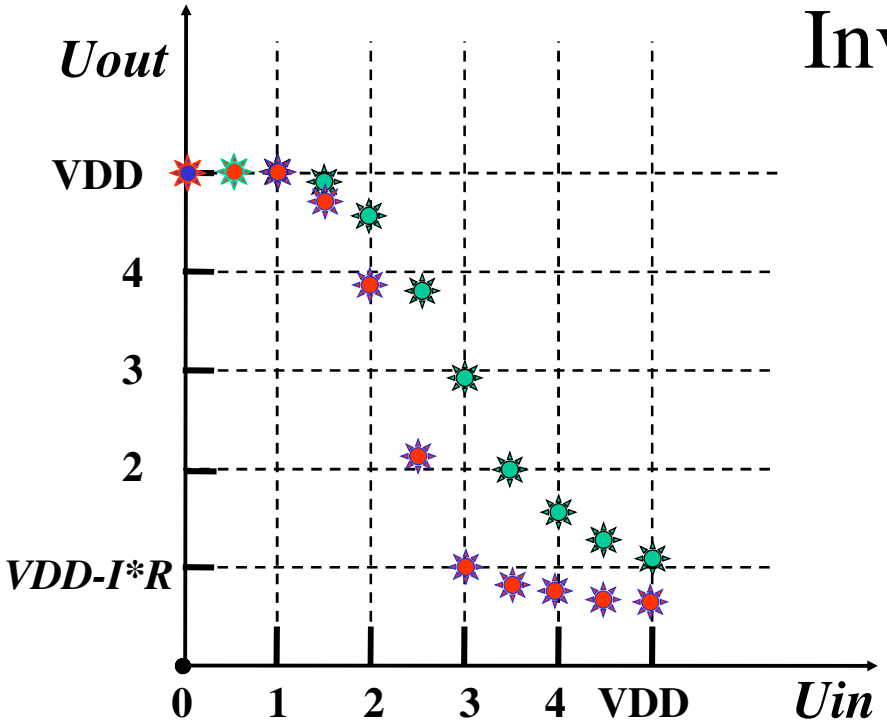
NMOS-Circuit technology



Inverter with resistance

- Depending on load elements different circuit technology
  - -Resistance
  - -MOS-diode
  - -Current source

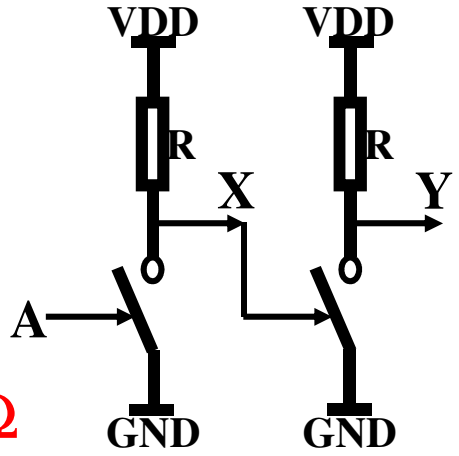
Inverter transfer characteristics

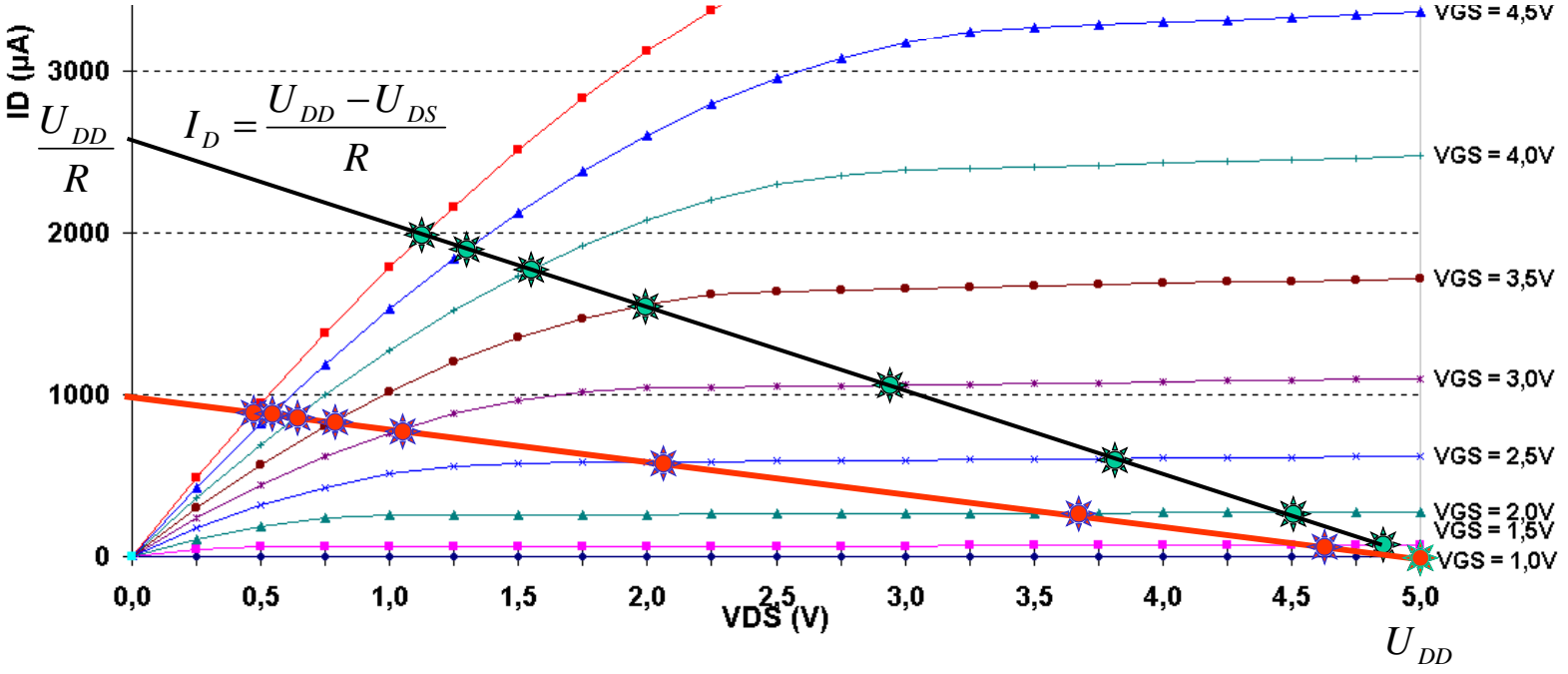


Poor design:

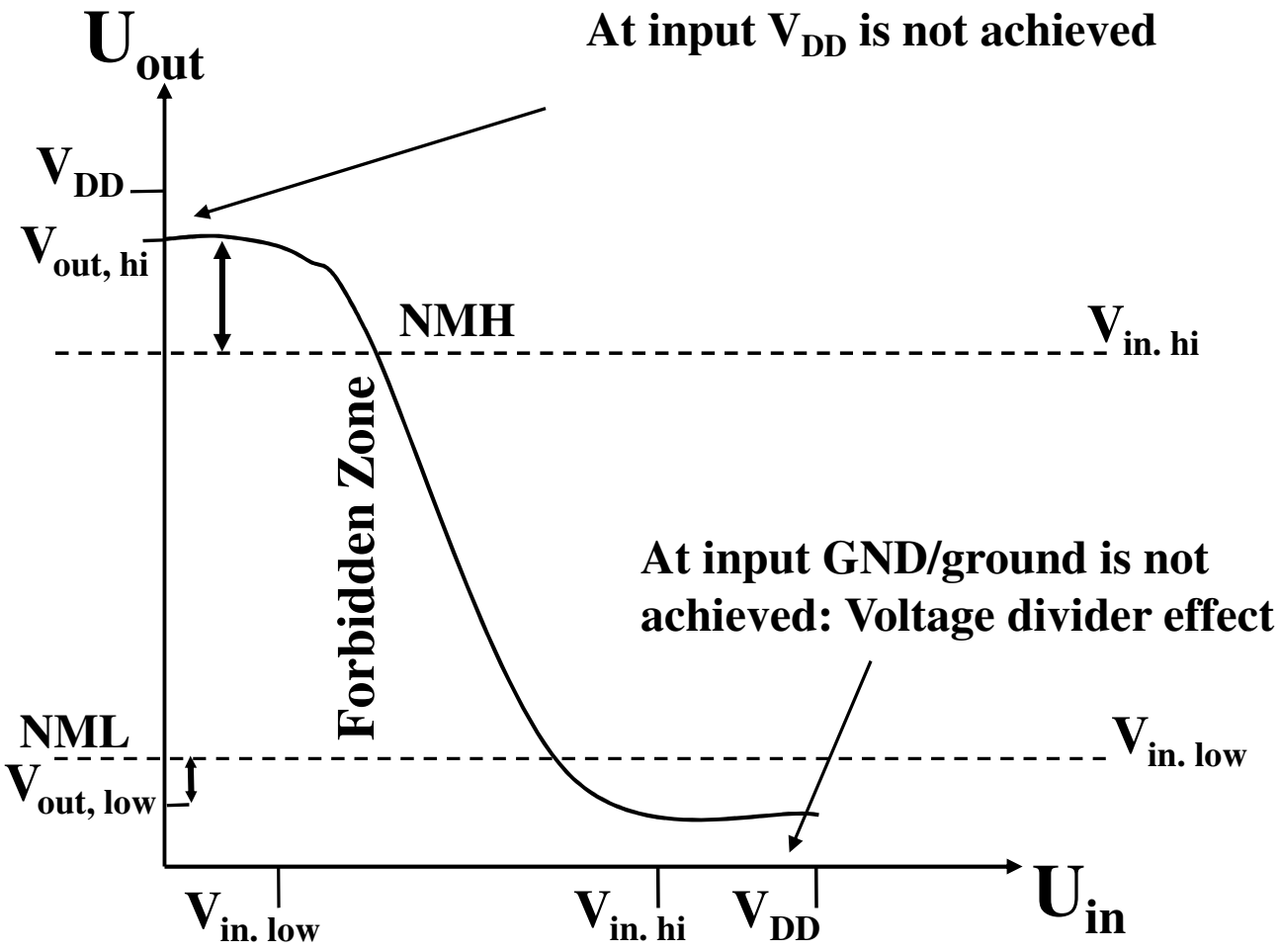
$V_{out,low} > V_T$

R: 2kΩ 5kΩ



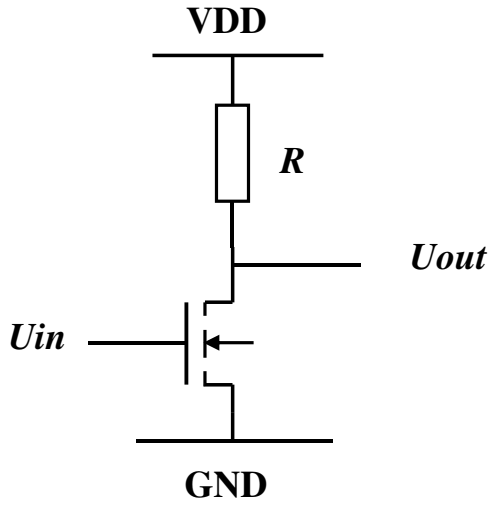


Noise Margin



Charcteristic of an inverter

Digital MOS-Circuit technology



Inverter with resistance

- Depending on load element different circuit technology
  - -resistance
  - -MOS-Diode
  - -Current source

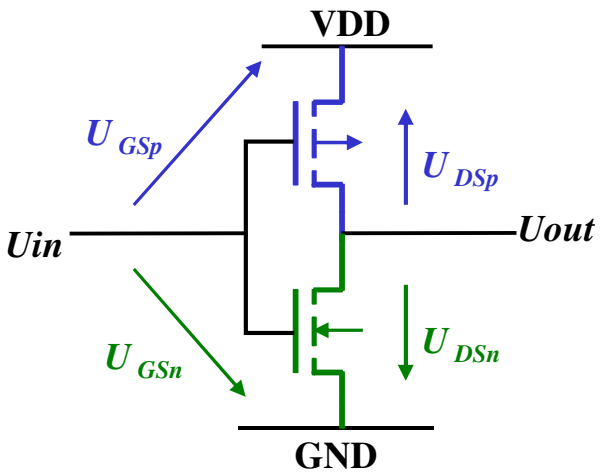
Disadvantage: with Uin = high, there is always a current flowing;
Uout is not ground

Solution: CMOS

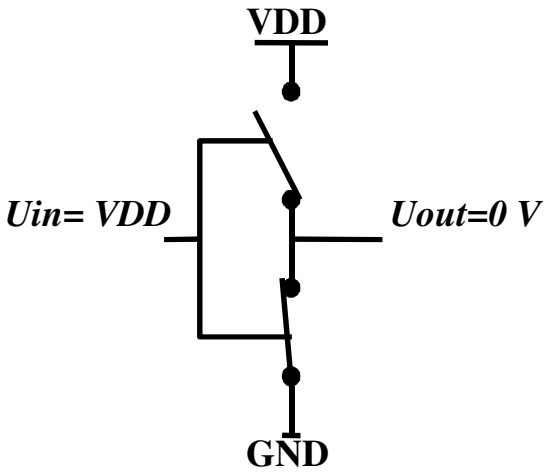
Chpater 4 Contents

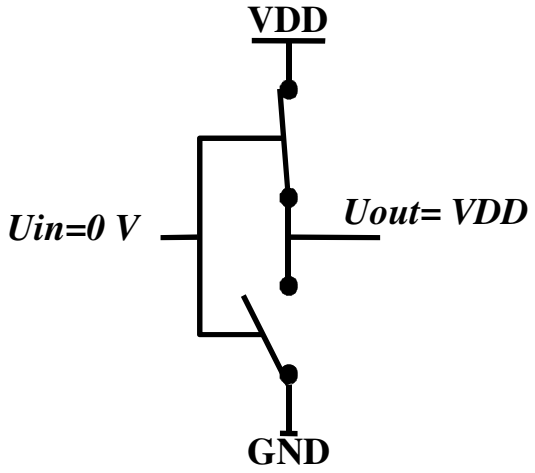
- Introduction Digital circuit technology
- Digital MOS-circuits
- CMOS - complementary MOS
- Pseudo-NMOS (p-channel-transistor as load)
- Delay times
- Power loss

CMOS-Complementary MOS



CMOS-Inverter

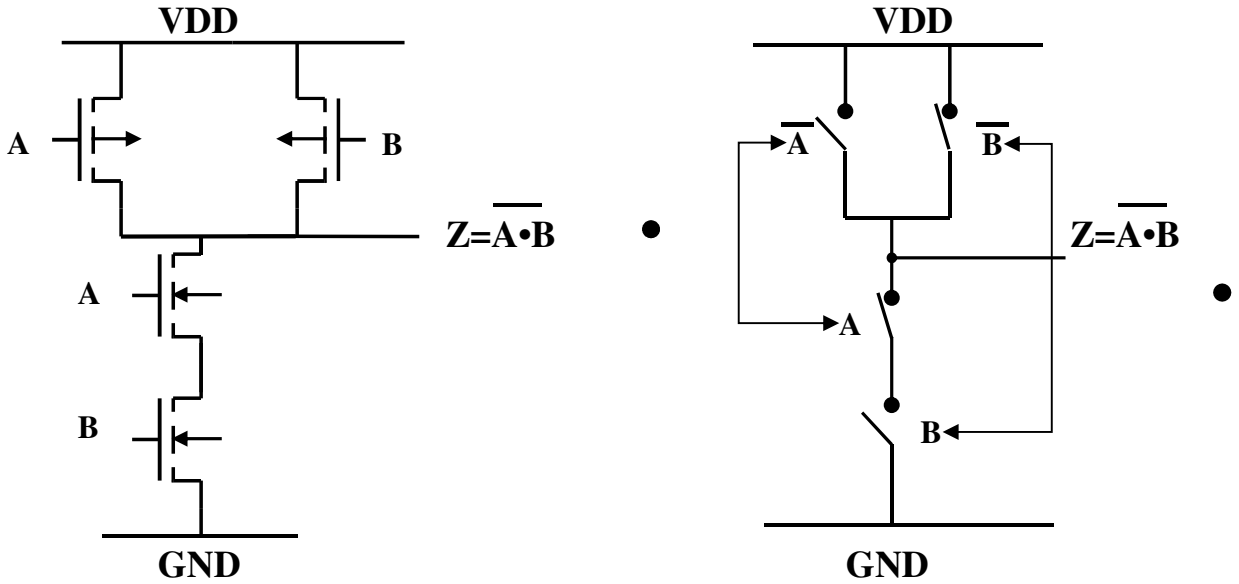




Switch Representation of CMOS-Inverter

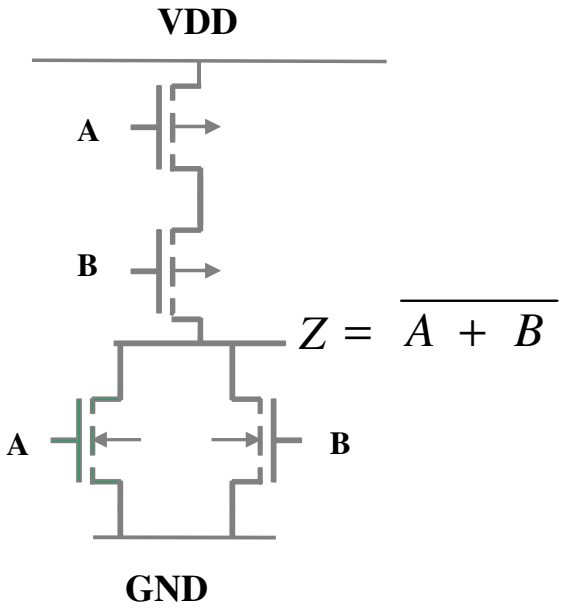
PMOS can be regarded as the load of NMOS.
Or vice versa: NMOS is the load of PMOS.
It is active load, as Ugs of load is changing.

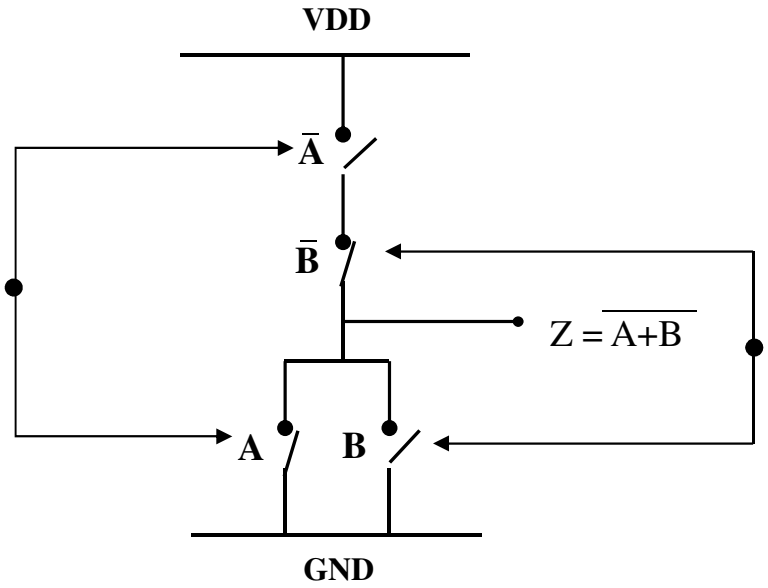
Realization of a NAND-Gate in CMOS



A	B	Z
1	1	0
0	1	1
1	0	1
0	0	1

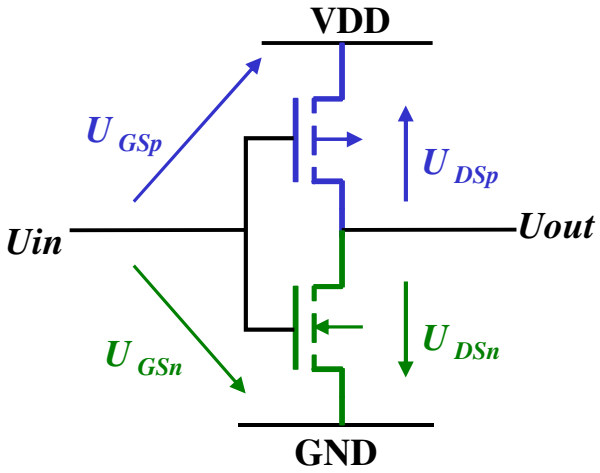
Realization of a NOR-Gate in CMOS



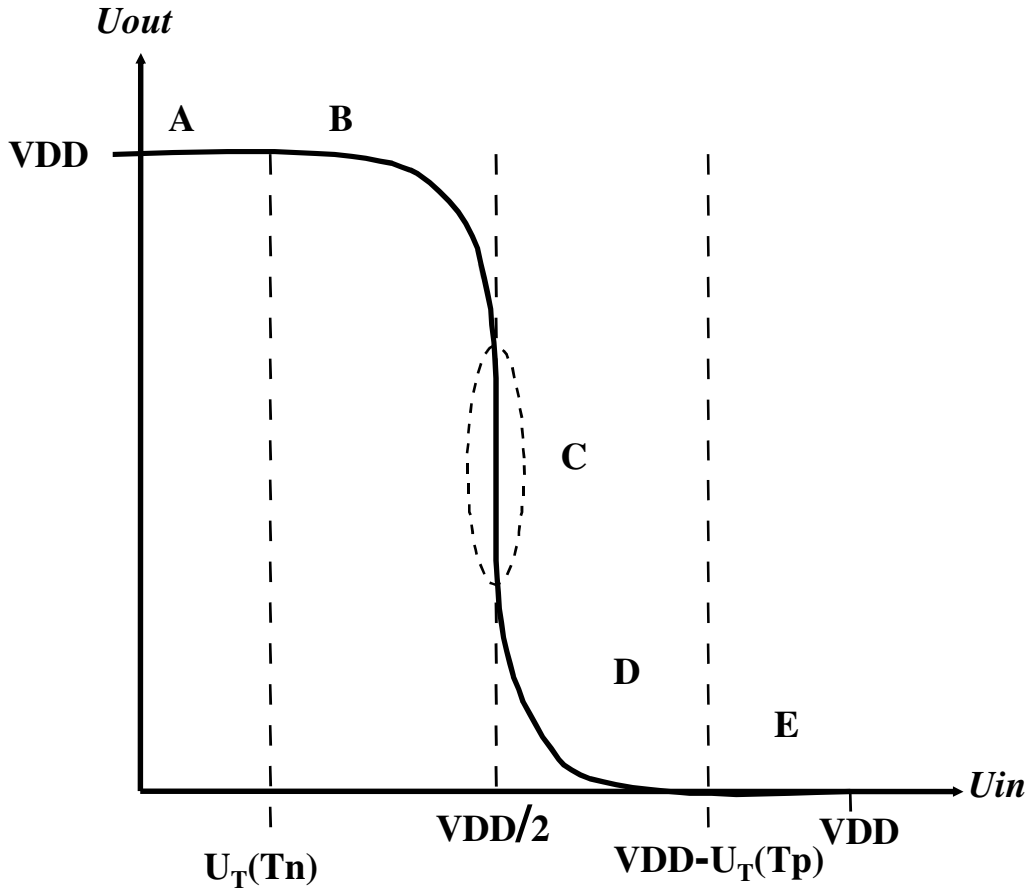


A	B	Z
1	1	0
0	1	0
1	0	0
0	0	1

Close view of the transfer characteristic of a CMOS-Inverter



CMOS-Inverter

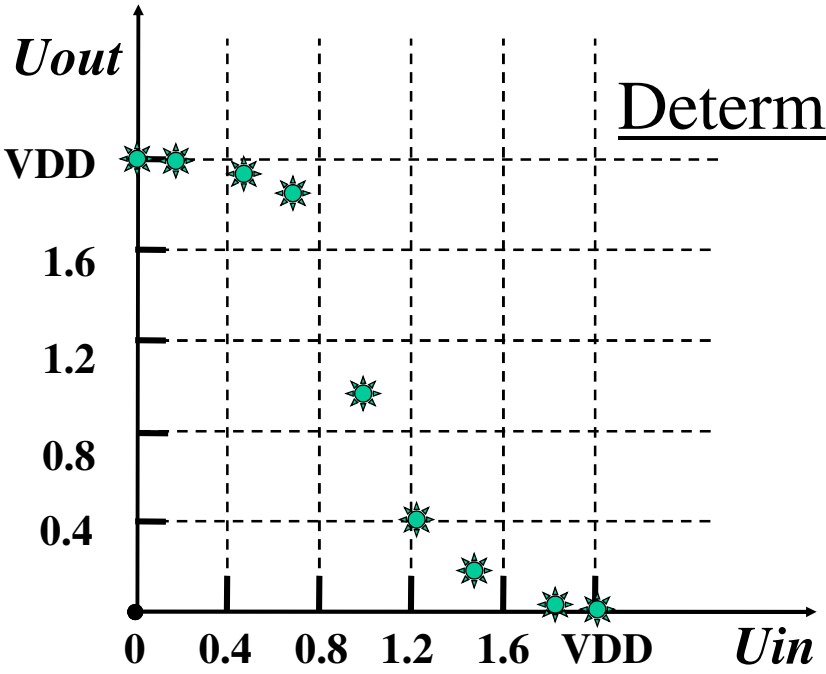


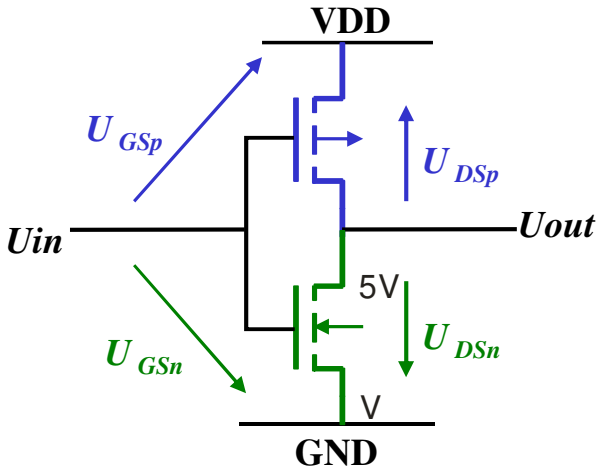
$$I_{Dn} = I_{Dp}$$

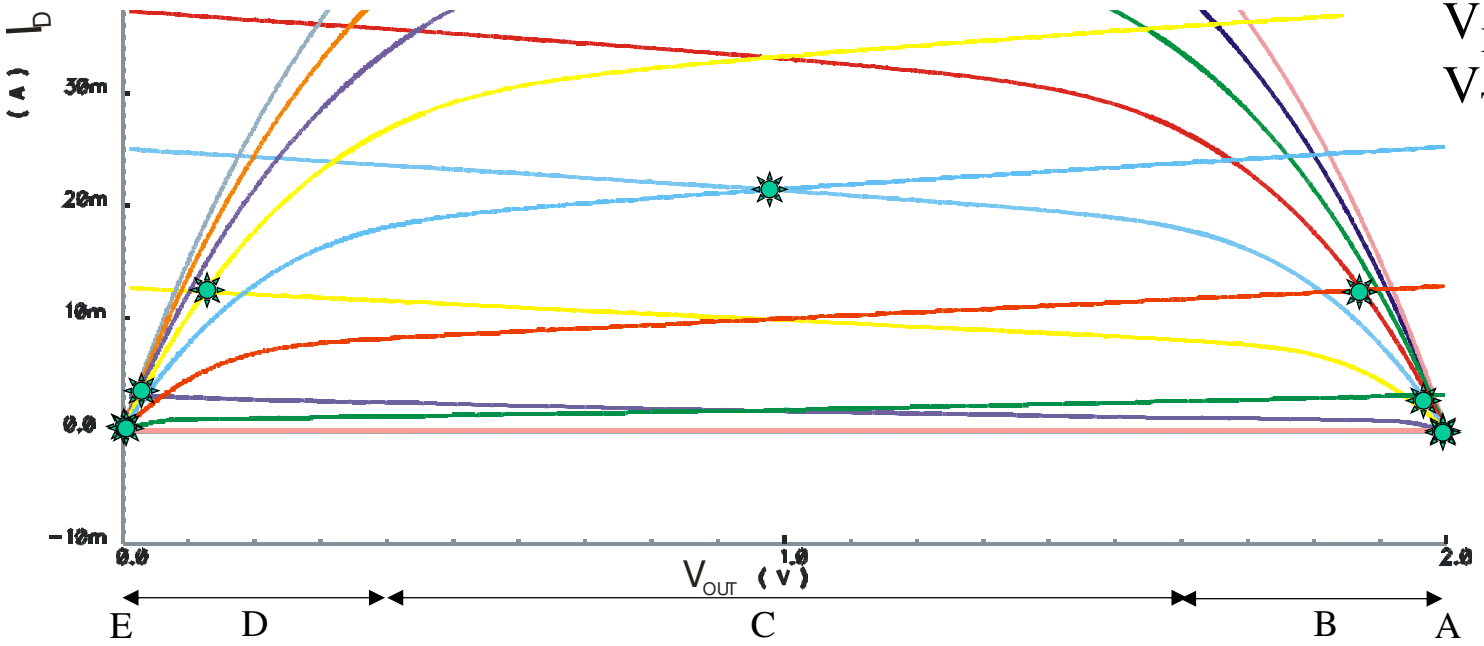
$$U_{GSn} = U_{in} \qquad U_{GSp} = |V_{DD} - U_{in}|$$

$$U_{DSn} = U_{out} \qquad U_{DSp} = |V_{DD} - U_{out}|$$

Determining CMOS-Inverter-Characteristic







$V_{DD} = 2V$

$V_{TN} = V_{TP} = 0{,}4\ V$

$V_{GS} = 1V$

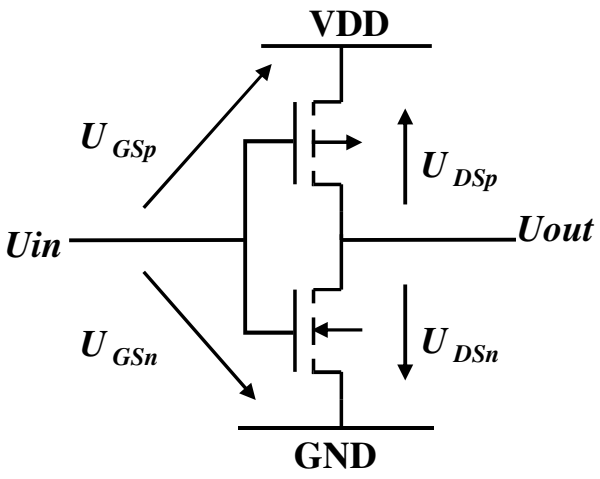
$V_{GS} = 0.75V$

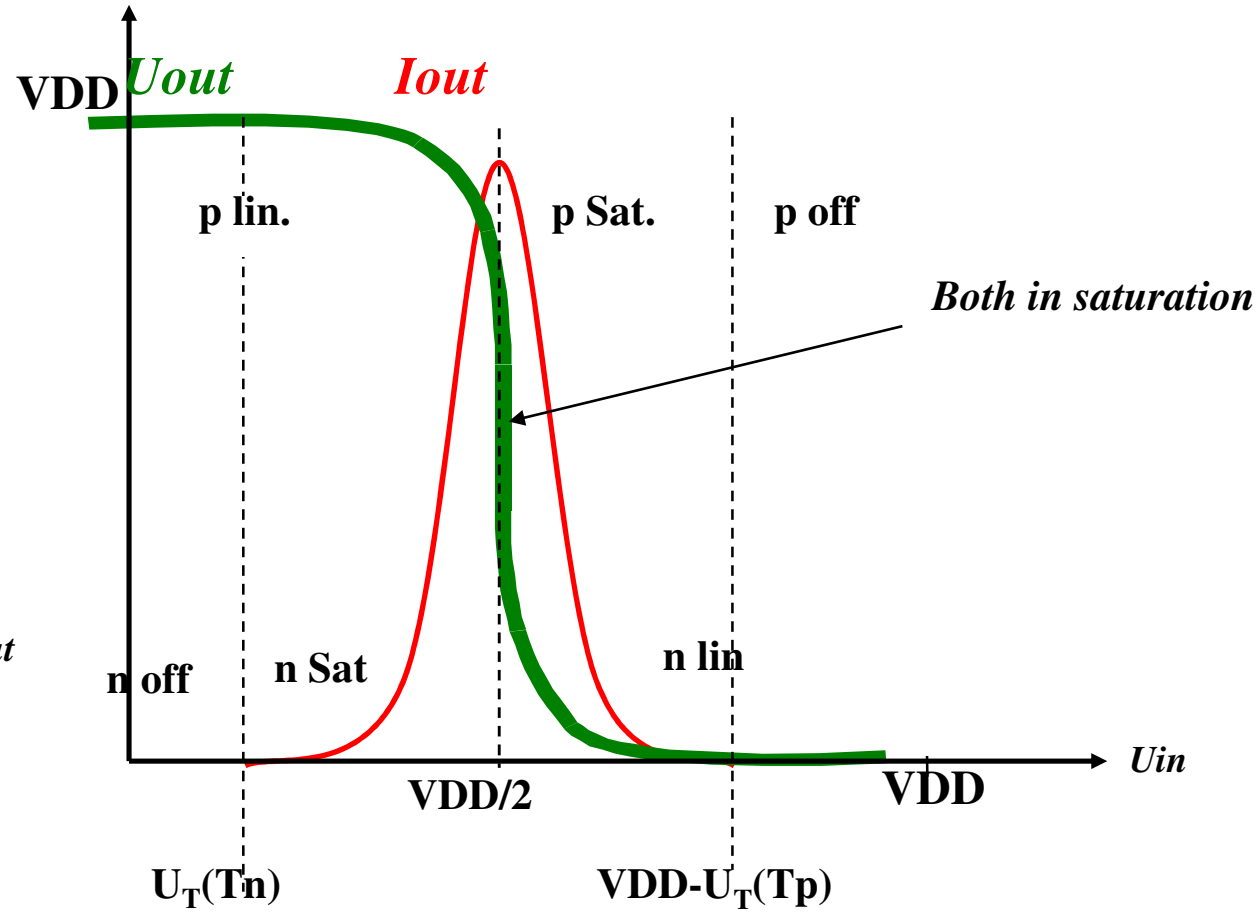
$V_{GS} = 0.5V$

$V_{GS} = 0.25V$

$V_{GS} = 0V$

Currrent of a CMOS-Inverter

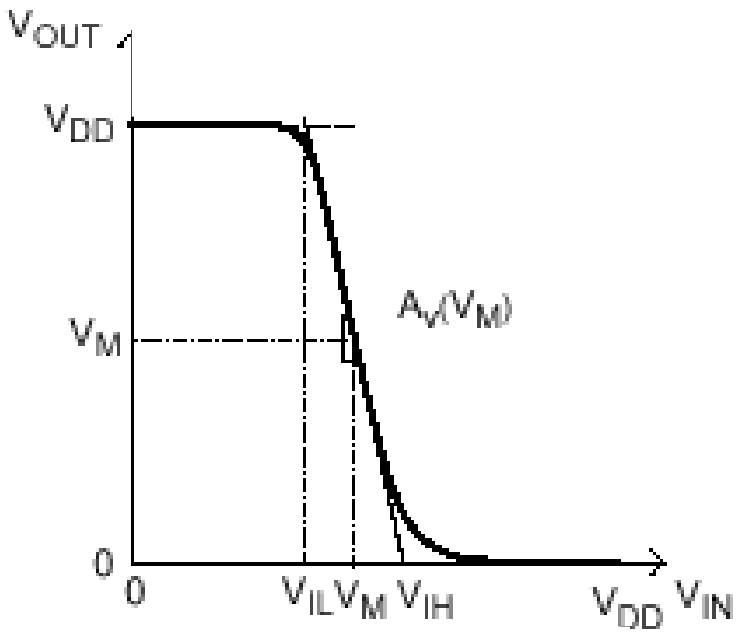




Transfer characteristic

- There is no static current;
- Output level always „clean“ on high or low
- During the transition there is a short circuit current

Noise Margin calculation for CMOS-Inverter



Definition:

$V_M = V_{IN} = V_{OUT}$

A_V: Gain

$V_{IN} \leq V_{IL} \Rightarrow V_{OUT} = \text{High}$

$V_{IN} \geq V_{IH} \Rightarrow V_{OUT} = \text{Low}$

V_M Calculation for CMOS-Inverter

$$I_{DN} = \frac{\beta_N}{2} \cdot (V_M - V_{TN})^2$$

$$|I_{DP}| = \frac{\beta_P}{2} \cdot (V_{DD} - V_M - |V_{TP}|)^2$$

$$I_{DN} = |I_{DP}|$$

$$V_M = \frac{V_{TN} + \sqrt{\beta_P / \beta_N} \cdot (V_{DD} - |V_{TP}|)}{1 + \sqrt{\beta_P / \beta_N}}$$

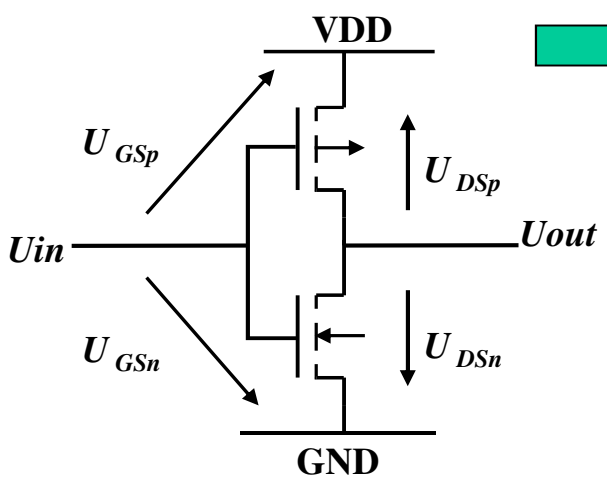
Common designs are symmetric.

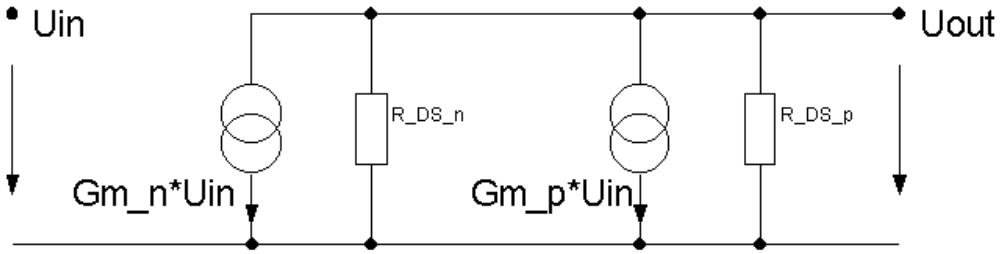
$\Rightarrow \beta_P \approx \beta_N$ ($W_P \approx 3 * W_N$)

$V_{TP} = V_{TN}$

$V_M = V_{DD} / 2$

Calculation of A_V and Noise Margin for CMOS-Inverter



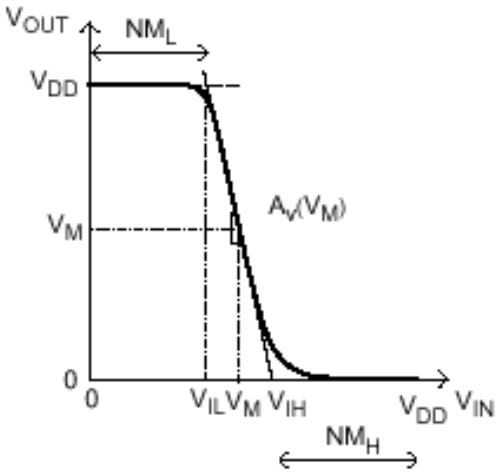


Small Signal-Equivalent circuit diagram

$$A_V = -\frac{g_{mn} + g_{mp}}{g_{DSn} + g_{DSp}}$$

Operation point is V_M / V_M (in, out).

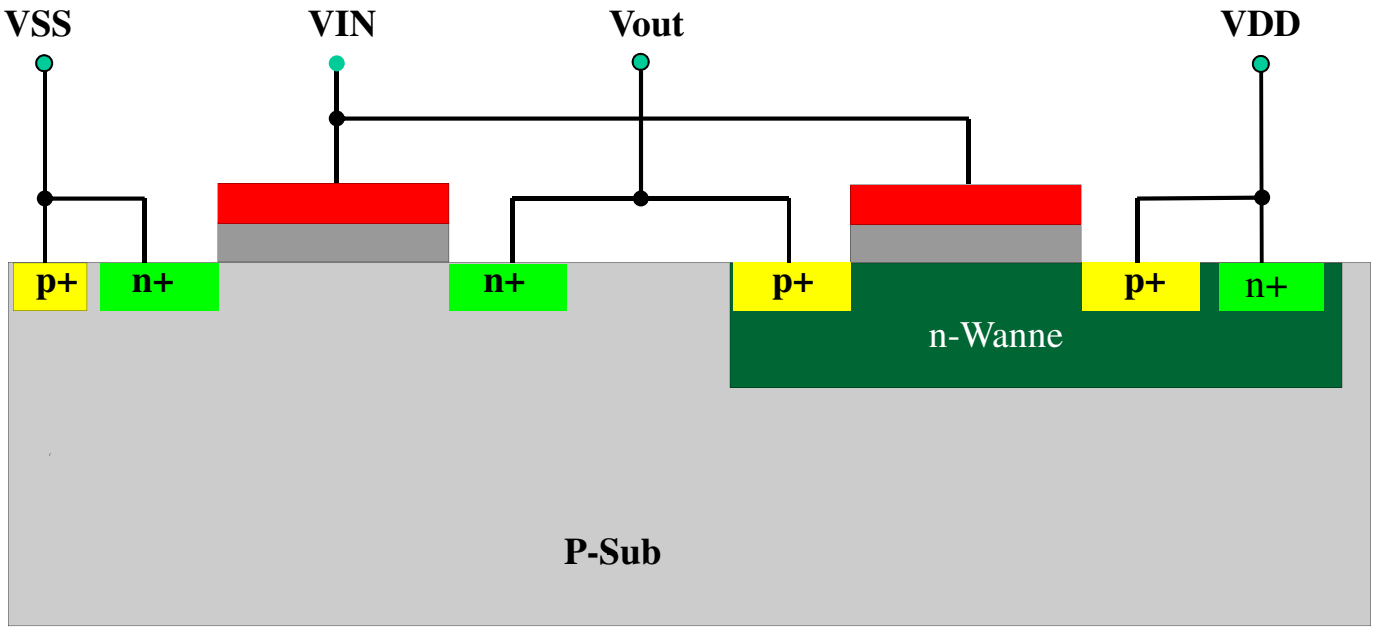
A_V is twice as large as that of inverter with current source



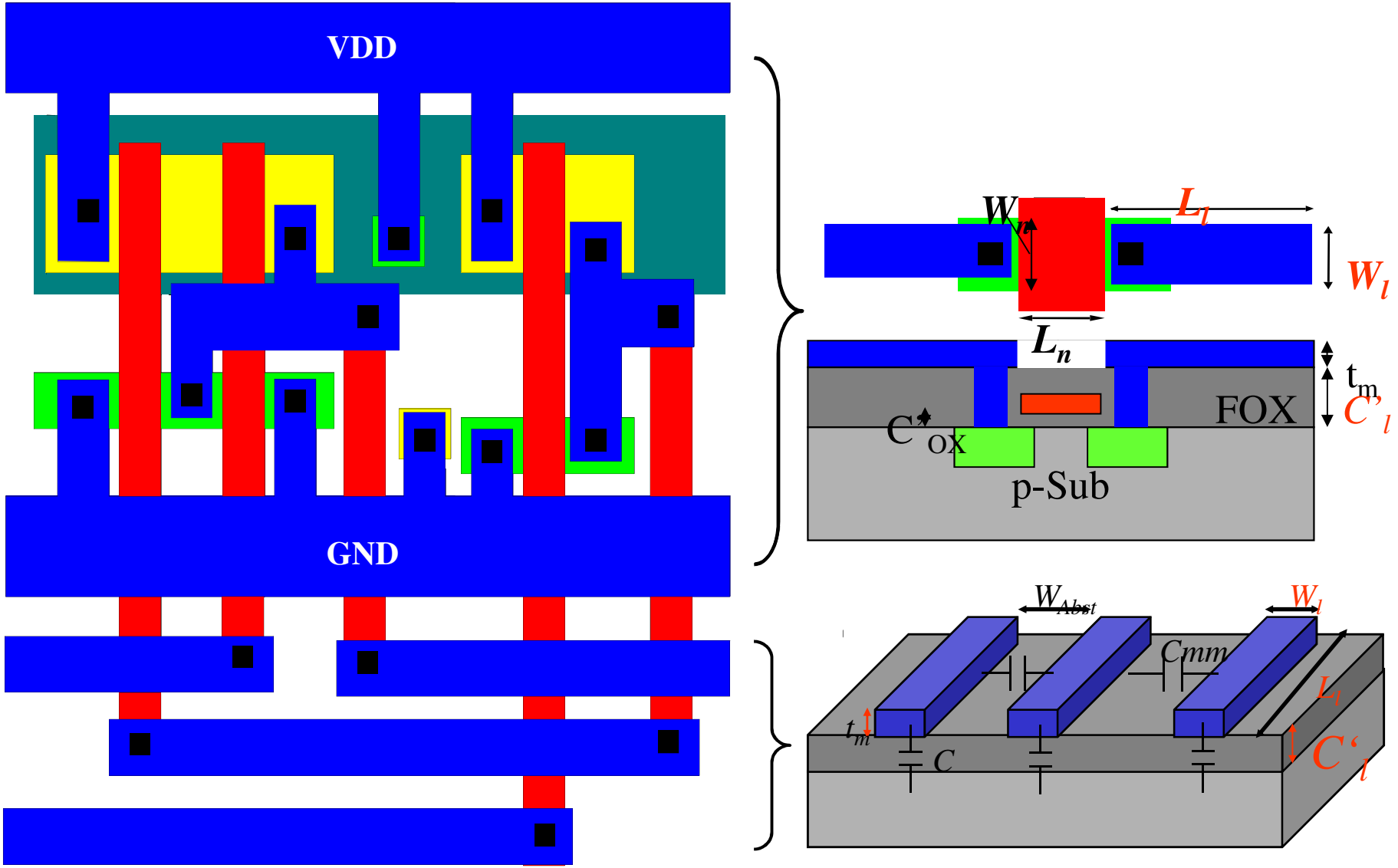
$$NM_L = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_V|}$$

$$NM_H = V_{DD} - V_{IH} = V_{DD} - V_M\left(1 + \frac{1}{|A_V|}\right)$$

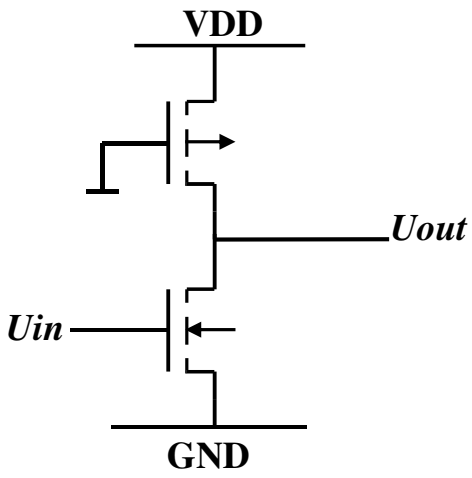
Implementation of CMOS-Inverter in a wafer process



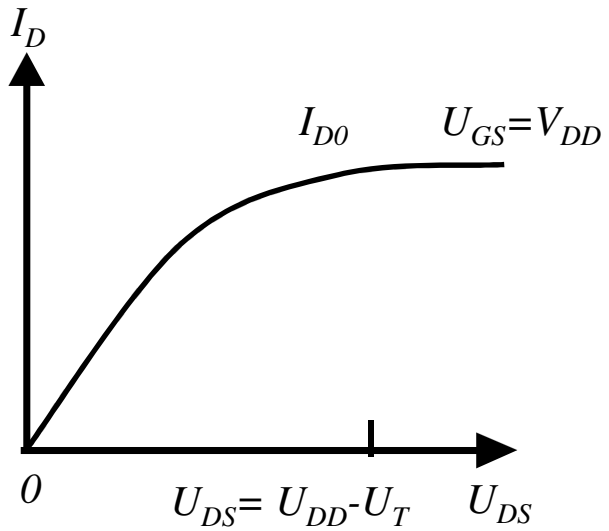
Layout

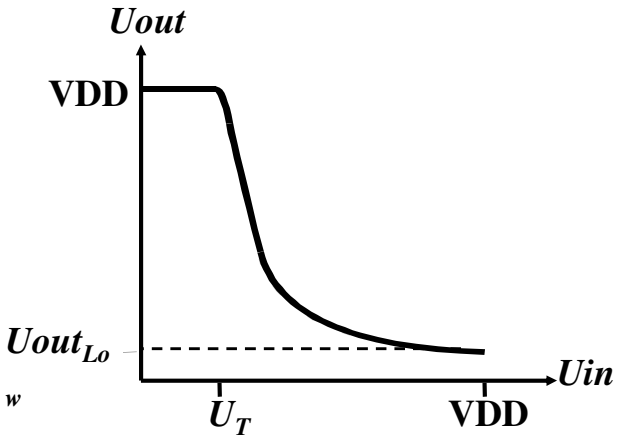


Pseudo-NMOS: P-Channel Transistor as Load



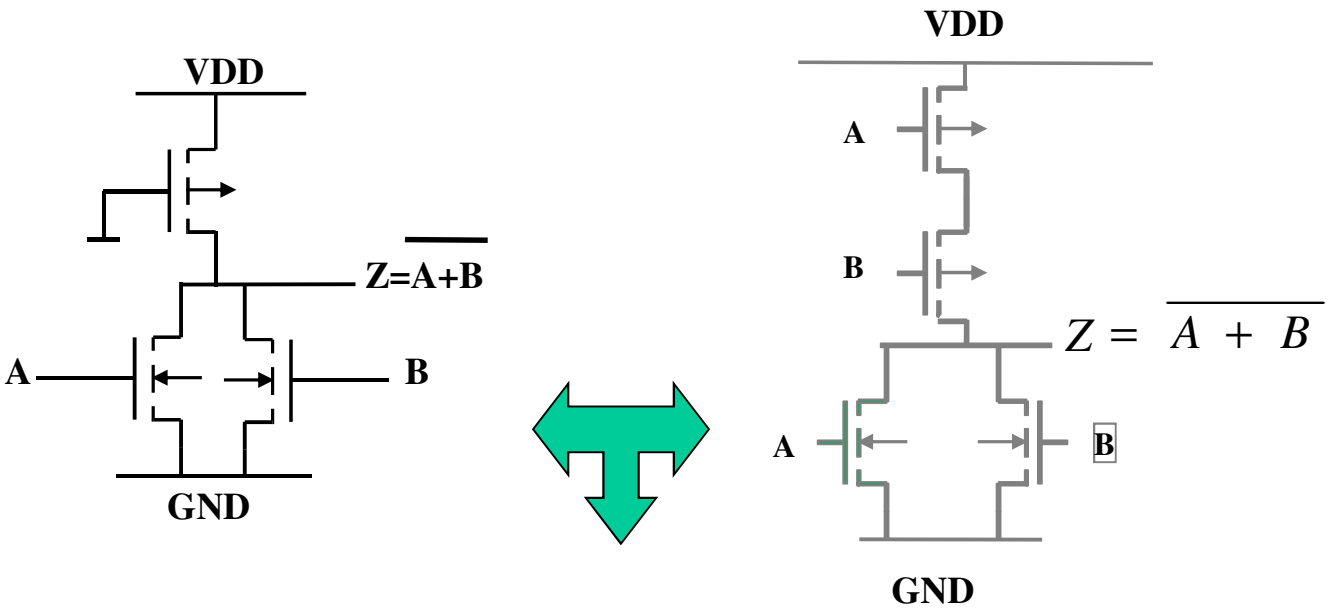
Pseudo-NMOS-Inverter





Transfer characteristics

Pseudo-NMOS-NOR



Disadvantage: DC current at Low

Advantages over standard CMOS NOR:

Lower size and higher speed

particularly with NOR with many inputs.

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