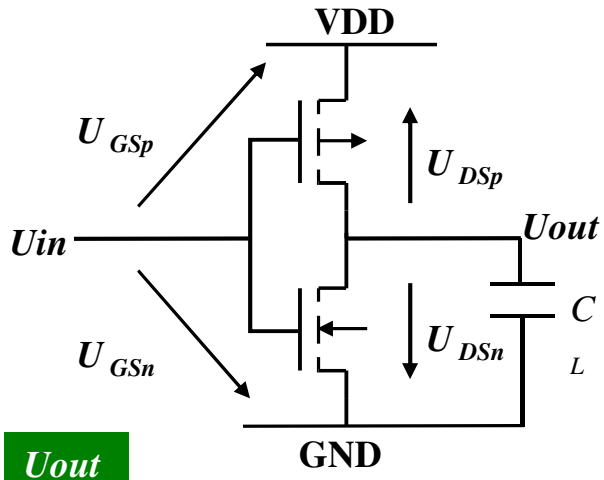
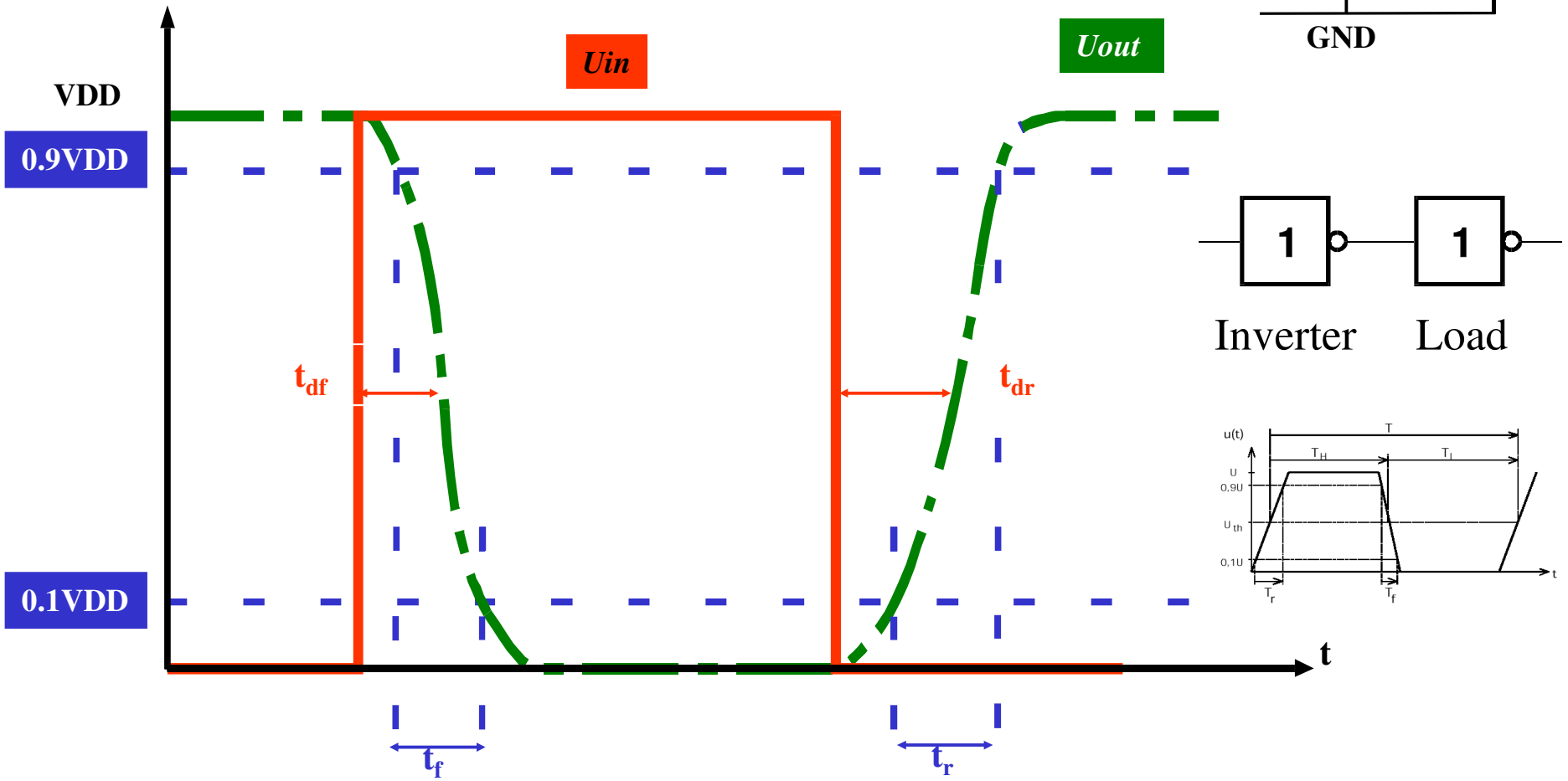
Chapter 4 Contents

- Introductioin digital circuitry
- Digital MOS-circuits
- CMOS - complementary MOS
- Pseudo-NMOS (p-channel-transistor as load)
- Delays
- Power Consumption

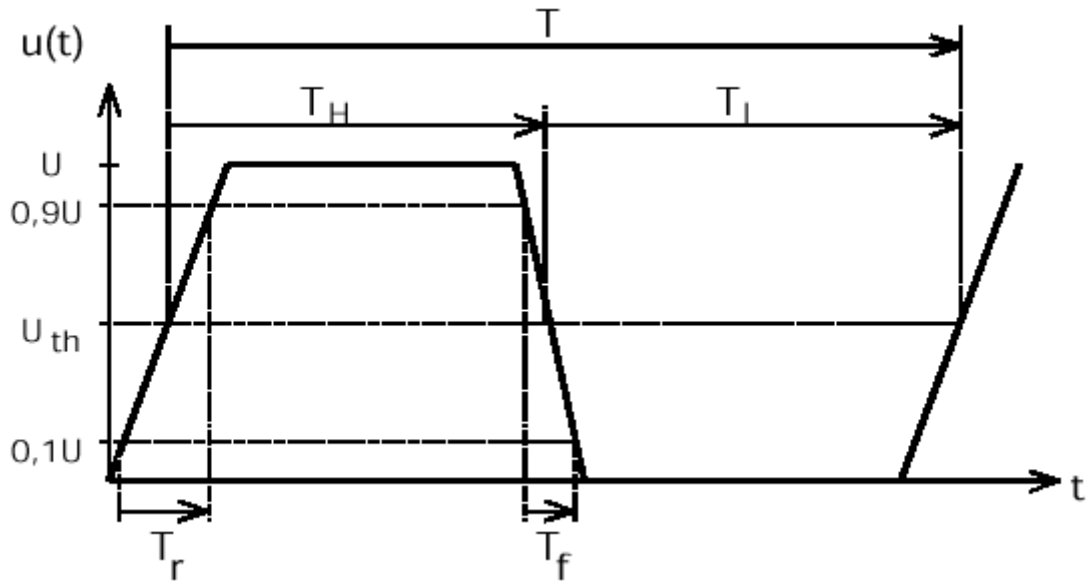
Definition of delay times

Charging of a load (capacity) via inverter





Simplified representation of a pulse signal



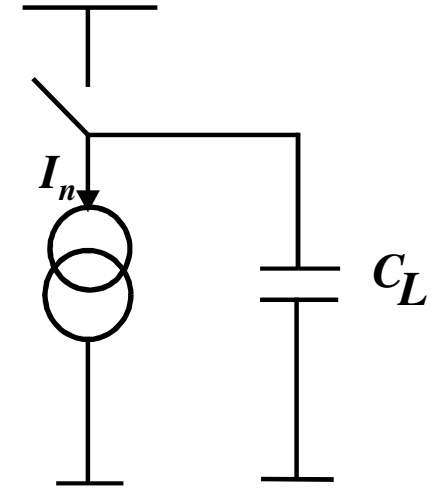
$U < 0.1 \cdot U_{DD}$ = Low ($U_{TN} = 0.2 \cdot U_{DD}$)

$U > 0.9 \cdot U_{DD}$ = High ($U_{TP} = 0.2 \cdot U_{DD}$)

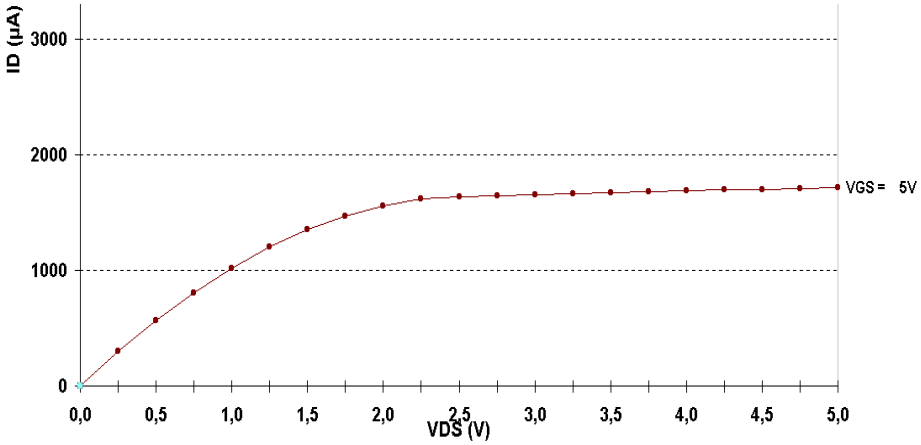
Period from $U = 0.1 \cdot U_{DD}$ to $0.9 \cdot U_{DD}$: T_R (rise time)

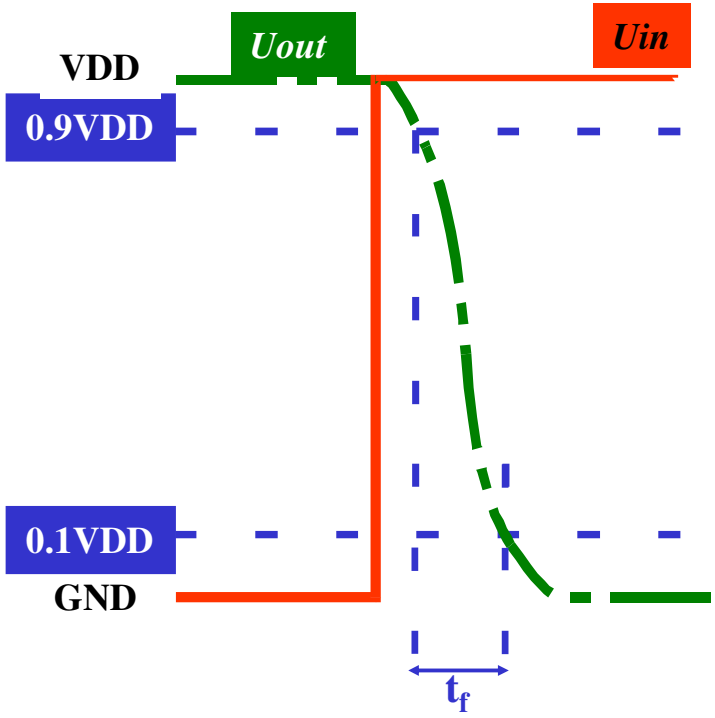
Period from $U = 0.9 \cdot U_{DD}$ to $0.1 \cdot U_{DD}$: T_F (fall time)

Delay times (Falling Edge)



$$I_n = -C_L \frac{dU_{OUT}}{dt}$$





$$t_f = \int_{t1}^{t2} dt = -\int_{0.9U_{DD}}^{0.1U_{DD}} \frac{C_L}{I_n} dU_{OUT}$$

1. n-channel-transistor in saturation:

$$I_n = \frac{\beta}{2}(U_{GS} - U_T)^2$$

2. n-channel-transistor in linear region:

$$I_n = \beta(U_{GS} - U_T - \tfrac{1}{2}U_{DS})U_{DS}$$

Discharge of capacity

1. $\Rightarrow$ n-Kanal-Transistor in Saturation $\Rightarrow$

$$t_{fs} = -\int_{0.9U_{DD}}^{U_{DD}-U_T} \frac{C_L}{I_n} dU_{OUT}$$

$$= \frac{C_L}{\frac{1}{2}\beta_n (U_{DD} - U_T)^2} (U_T - 0.1U_{DD})$$

2. $\Rightarrow$ n-channel-transistor in linear range $\Rightarrow$

$$\Rightarrow t_{fl} = -\int_{U_{DD}-U_T}^{0.1U_{DD}} \frac{C_L}{I_n} dU_{out}$$

$$= \frac{C_L}{\beta_n (U_{DD} - U_T)} \ln\left(\frac{19U_{DD} - 20U_T}{U_{DD}}\right)$$

Falling Edge

$$t_{fs} = \frac{2C_L}{\beta_n (U_{DD} - U_T)^2} (U_T - 0.1U_{DD})$$

$$t_{fl} = \frac{C_L}{\beta_n (U_{DD} - U_T)} \ln\left(\frac{19U_{DD} - 20U_T}{U_{DD}} \right)$$

$$\left.\begin{array}{ll} U_{DD} = 5V & U_T = 1V \\ U_{DD} = 3,3V & U_T = 0,65V \\ U_{DD} = 1,8V & U_T = 0,35V \end{array}\right\} \Rightarrow U_T \approx \frac{1}{5} U_{DD}$$

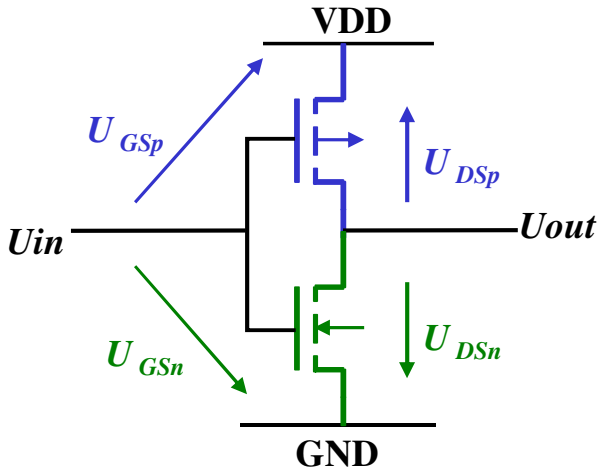
$$t_f = t_{fs}(0.9 \cdot U_{DD} \rightarrow U_{DD} - U_T) + t_{fl}(U_{DD} - U_T \rightarrow 0.1 \cdot U_{DD})$$

$$\approx \frac{0.3 \cdot C_L}{\beta_n U_{DD}} + \frac{3.4 \cdot C_L}{\beta_n U_{DD}} \approx \frac{4C_L}{\beta_n U_{DD}}$$

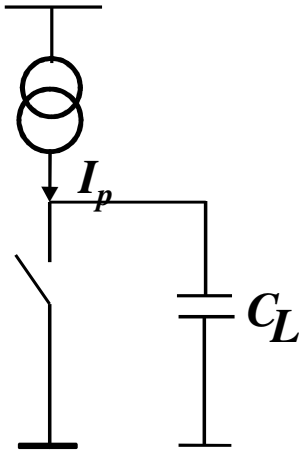
Charging of a capacity

Falling edge:

$$t_f = t_{fl} + t_{fs} \approx \frac{4C_L}{\beta_n U_{DD}}$$



Rising Edge:



$$t_r = t_{rl} + t_{rs} \approx \frac{4C_L}{\beta_p U_{DD}}$$

For higer speed: $C_L \downarrow \quad U_{DD} \uparrow \quad \beta \uparrow \quad \left(\beta = \frac{W}{L} \mu C_{ox}^{'} = \frac{W}{L} \mu \frac{\varepsilon_{ox}}{t_{ox}} \right)$

Total delay times

$$t_{ges} = t_r + t_f$$

$$= \frac{4C_L}{U_{DD}\beta_n} + \frac{4C_L}{U_{DD}\beta_p}$$

$$t_{ges} = \frac{4C_L}{U_{DD}}\left(\frac{1}{\beta_n} + \frac{1}{\beta_p}\right)$$

Particularly for $t_f = t_r$

$$\Rightarrow \beta_n = \beta_p = \beta \quad \left(= \frac{W}{L}\mu\frac{\varepsilon_{ox}}{t_{ox}}\right)$$

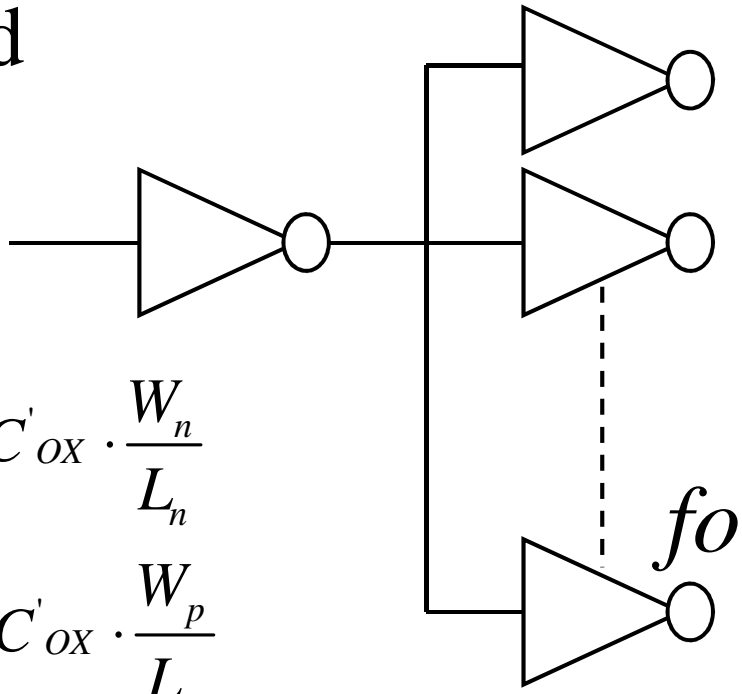
$$t_{ges} = t_r + t_f = \frac{8C_L}{U_{DD}\beta}$$

$$\Rightarrow bei\ L_n = L_p \quad , \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$$

$$\Rightarrow W_p \approx 3 * W_n$$

Delay times with inverter as load

$$t_{ges} = \frac{4C_L}{U_{DD}}\left(\frac{1}{\beta_n} + \frac{1}{\beta_p}\right)$$



$$\beta_n = \mu_n C'_{OX} \cdot \frac{W_n}{L_n}$$

$$C_{Linv} = (W_n L_n + W_p L_p) C'_{OX}$$

$$\beta_p = \mu_p C'_{OX} \cdot \frac{W_p}{L_p}$$

$$t_{ges} = 4\frac{C'_{OX} \cdot L \cdot (W_n + W_p)}{U_{DD}} \cdot \left(\frac{L}{W_n \mu_n C'_{OX}} + \frac{L}{W_p \mu_p C'_{OX}}\right)$$

Assumption :

$$L_n = L_p = L$$

If $t_r = t_f \Rightarrow W_n \mu_n = W_p \mu_p$

$$t_{ges} = 8\frac{L^2}{U_{DD}} \cdot \left(\frac{1}{\mu_n} + \frac{1}{\mu_p}\right)$$

fo (fan-out) inverters as load yield to: $t_{ges,fo} = fo * t_{ges}$

Minimum delay time (with inverter as load)

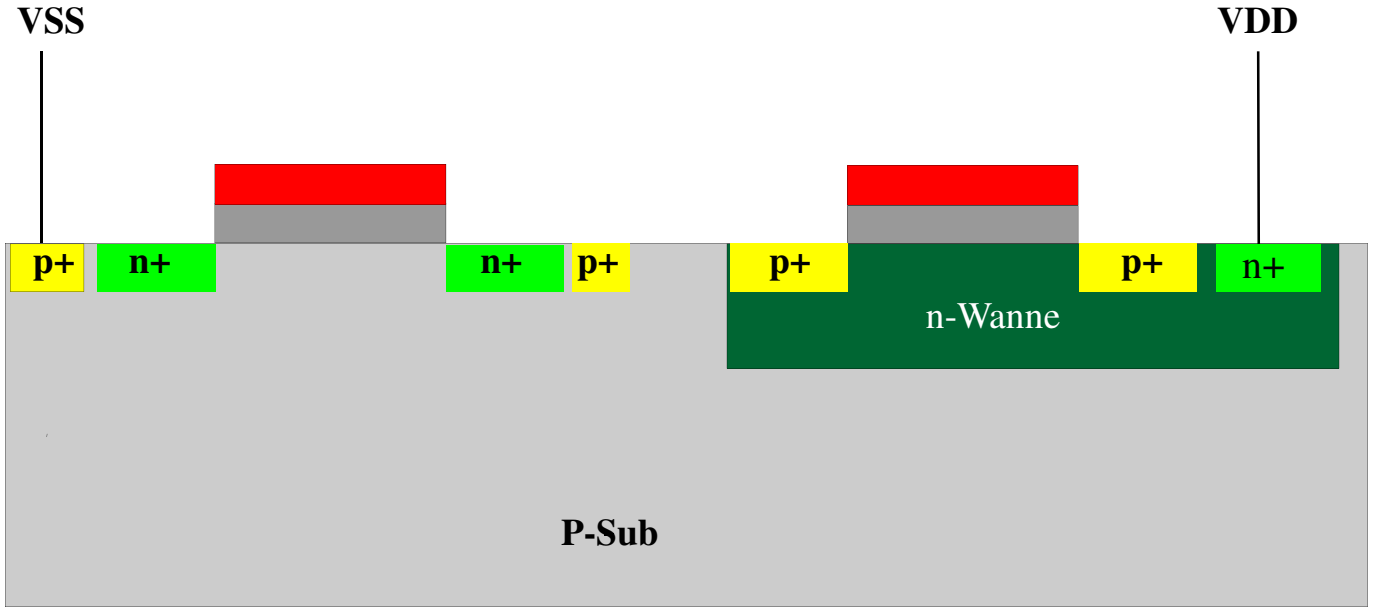
$$t_{ges} = \frac{4C_L}{U_{DD}}\left(\frac{1}{\beta_n}+\frac{1}{\beta_p}\right)$$

$$t_{ges} \text{ minimum} \Rightarrow \left.\frac{\mathrm{dt_{ges}}}{\mathrm{dW_p}}\right|_{W_n=const.} = 0$$

$$t_{ges} = 4\frac{L^2\cdot(W_n+W_p)}{U_{DD}}\cdot\left(\frac{1}{W_n\mu_n}+\frac{1}{W_p\mu_p}\right)$$

Solution: $\frac{W_p}{W_n} = \sqrt{\frac{\mu_n}{\mu_p}}$

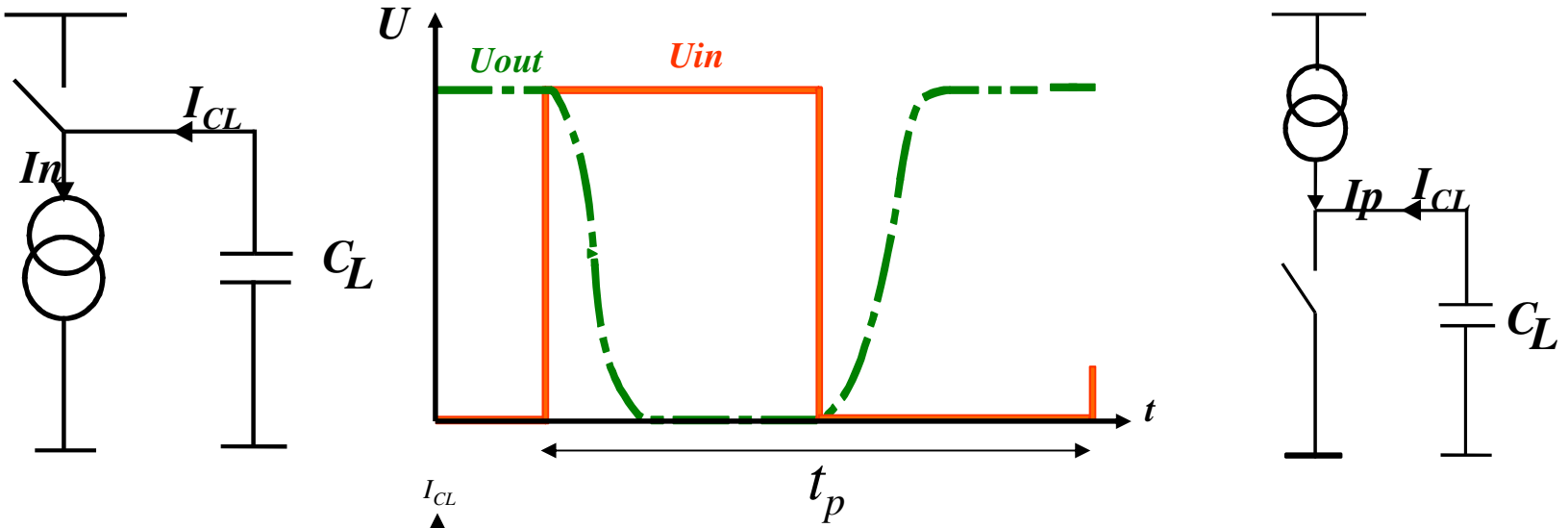
Static power loss



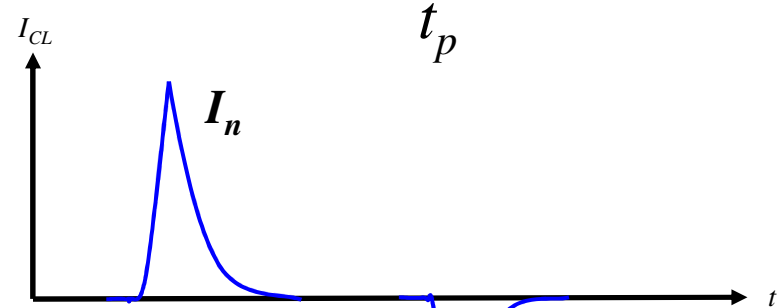
$$I_L = A \cdot I_s \left(e^{\left(\frac{U_D}{kT/q} \right)} - 1 \right) \qquad I_{WI} = I_{WIo} e^{n\left(\frac{U_{GS} - U_T}{kT/q} \right)}$$

$$P = \sum_n \left(I_L + I_{WI} \right) * U_{DD}$$

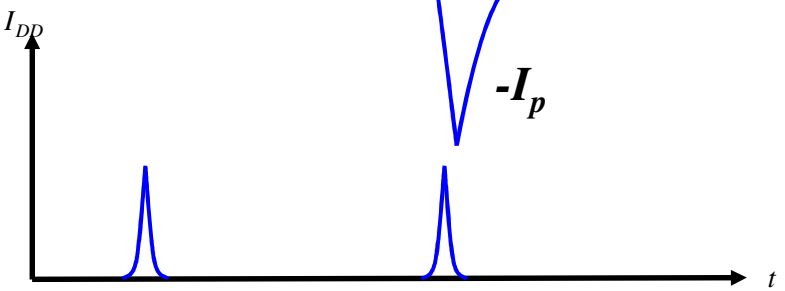
Dynamic power loss



Charging current



Capacity (90%)



Short circuit (9%)

Short circuit current

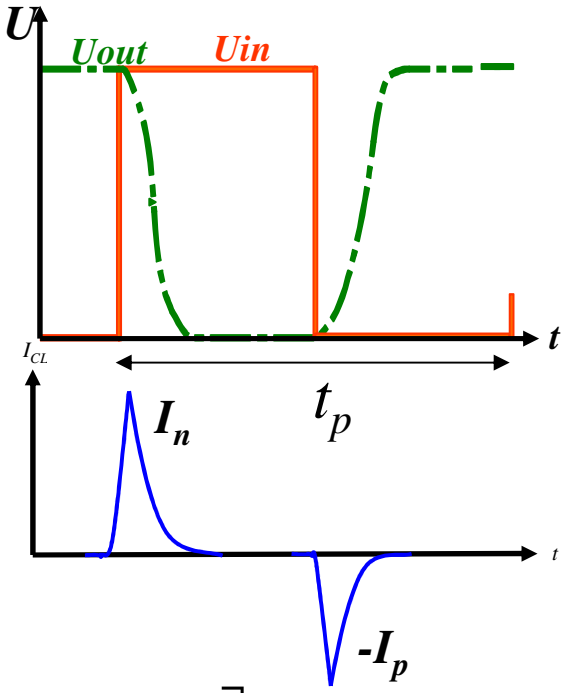
Static current (1%)

Average dynamic (C-load) power loss

$$P = \frac{1}{t_p}\left[\int_0^{t_p} I(t).U_{out}(t)dt\right]$$

$$i_n(t) = -C_L\frac{dU_{out}}{dt}$$

$$i_p(t) = -C_L\frac{d(U_{DD}-U_{out})}{dt}$$



$$P = \frac{1}{t_p}\left[\int_0^{t_r} i_p(t).(U_{DD}-U_{out}(t))dt + \int_0^{t_f} i_n(t).U_{out}(t)dt\right]$$

$$P = \frac{1}{t_p}\left[\int_0^{U_{DD}} -C_L(U_{DD}-U_{out})d(U_{DD}-U_{out}) + \int_{U_{DD}}^{0} -C_L U_{out}dU_{out}\right]$$

$$P = I\cdot U_{DD} = \frac{Q}{t_P}\cdot U_{DD} = \frac{C_L\cdot U_{DD}}{t_P}\cdot U_{DD} = \frac{C_L\cdot U_{DD}^2}{t_P} = f\cdot C_L\cdot U_{DD}^2$$

Power loss ⇔ Speed

$$P = \frac{C_L \cdot U_{DD}^2}{t_p} = f \cdot C_L \cdot U_{DD}^2$$

For low power circuitry: $f \downarrow \quad C_L \downarrow \quad U_{DD} \downarrow$

$$t_{ges} = \frac{4C_L}{U_{DD}} \left(\frac{1}{\beta_n} + \frac{1}{\beta_p} \right)$$

For high speed circuitry: $U_{DD} \uparrow \qquad C_L \downarrow \quad \beta \uparrow$

Example: a symetric inverter as load

$$t_{ges} = 8 \frac{L^2}{U_{DD}} \cdot \left(\frac{1}{\mu_n} + \frac{1}{\mu_p} \right) \qquad U_{DD} \uparrow \quad L \downarrow \quad (temp \downarrow)$$

Low Power and High Speed is contradiction.

Chapter 5

- Design rules
- Standard cell layout
- Scaling

Design Rules (Layout Design Rules)

Why Design Rules

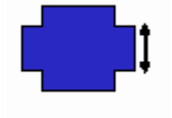
- fabrication process has minimum/maximum feature sizes that can be produced for each layer

- alignment between layers requires adequate separation (if layers unconnected) or overlap (if layers connected)

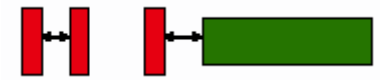
- proper device operation requires adequate separation

Basic Rules

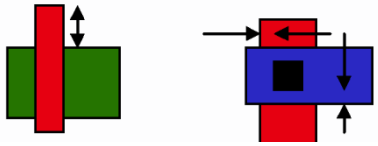
Minimum width



Minimum distance

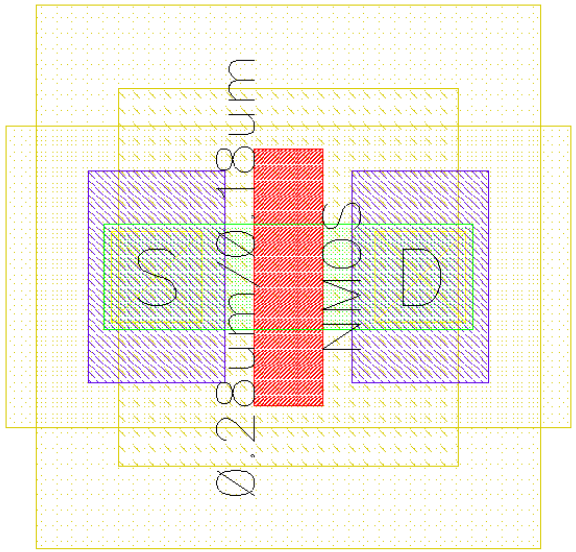


Minimum overlap

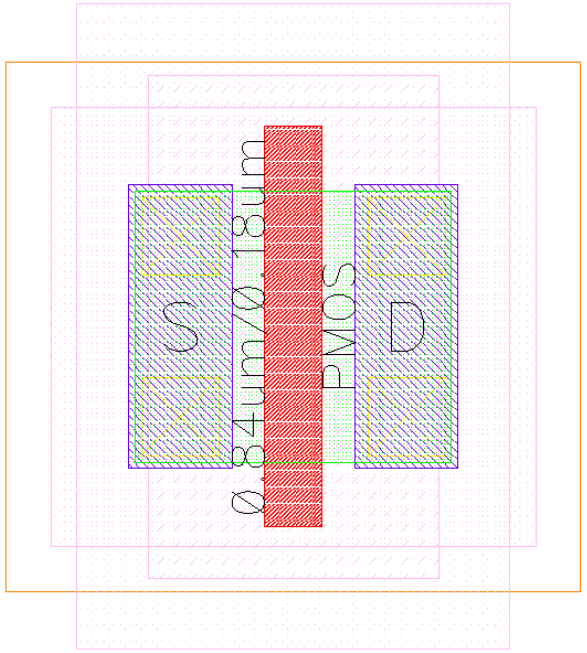


Hierarchically Layout

Polygom	->	Transistor (cell)
Transistor	->	Gate (cell)
Gate	->	Logical function
Logical function	->	Complex function
Complex function	->	Chip Top Level

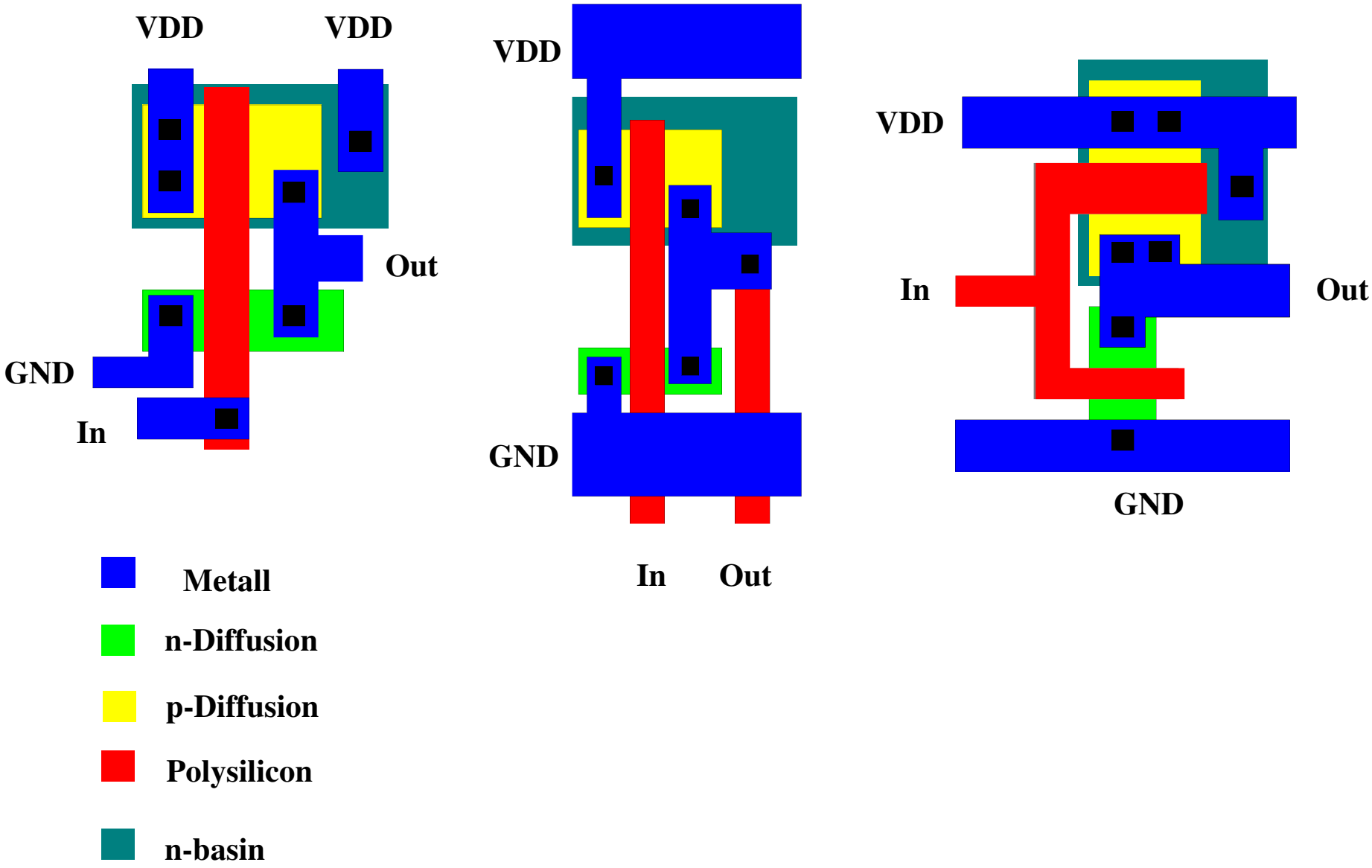


NMOS 0.28/0.18

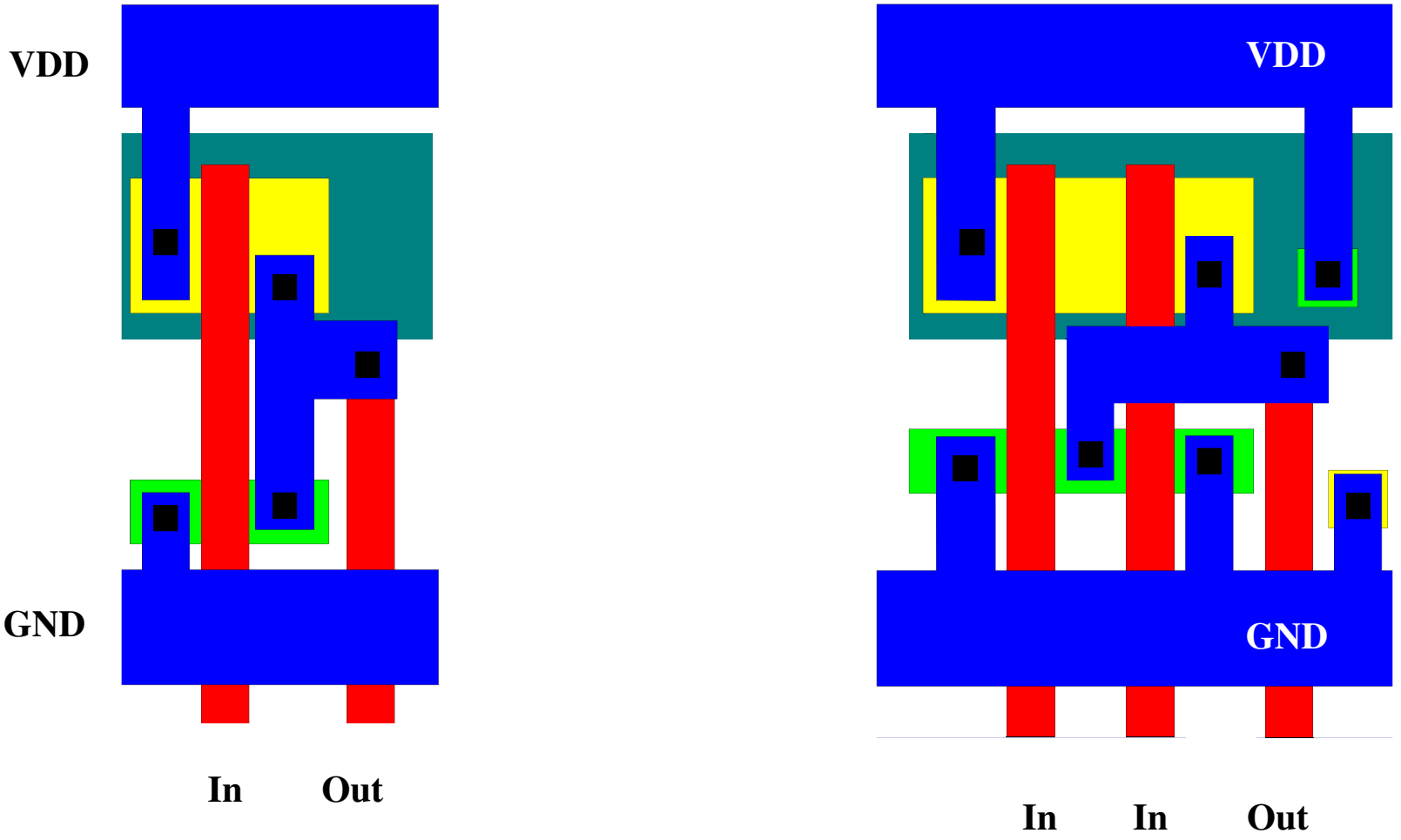


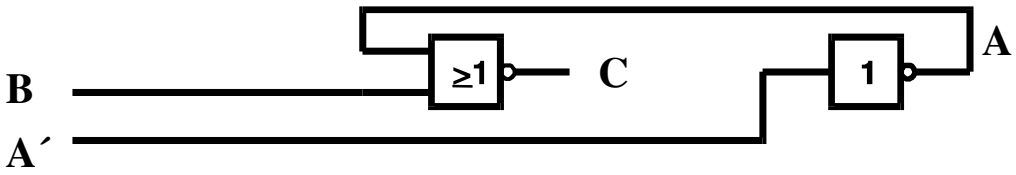
PMOS 0.84/0.18

Inverter Layouts

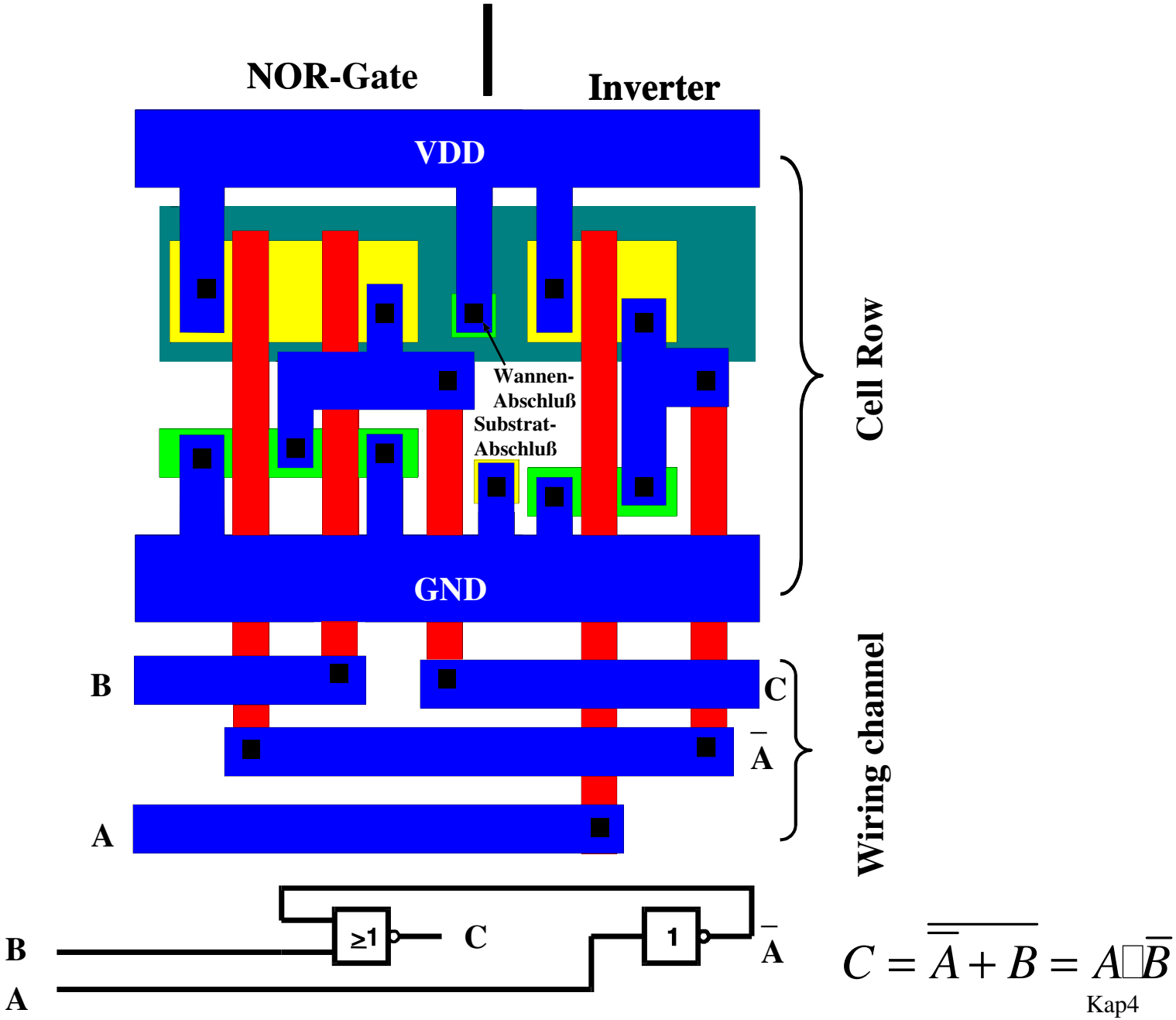


Layout of an NOR-Gate

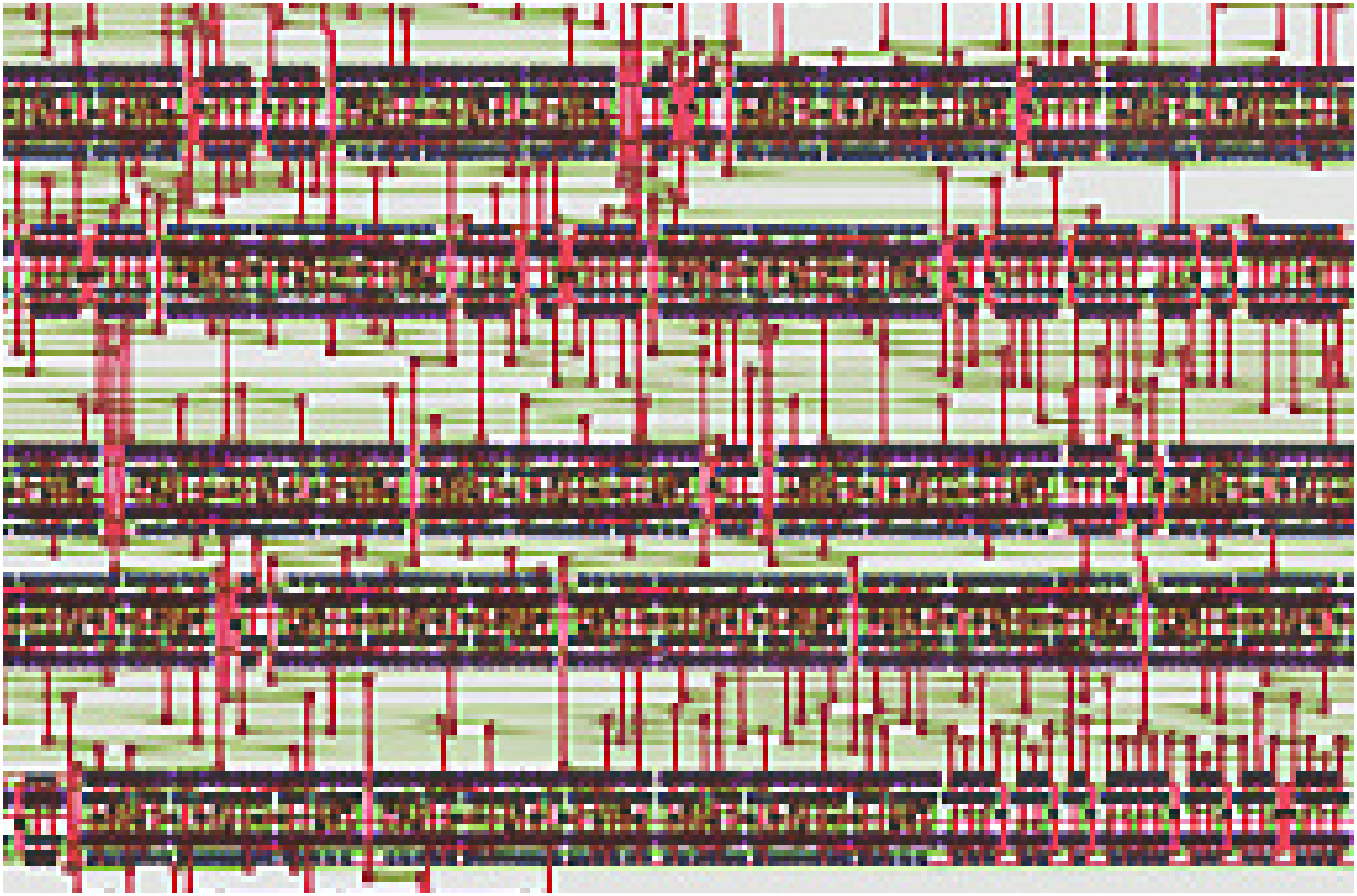




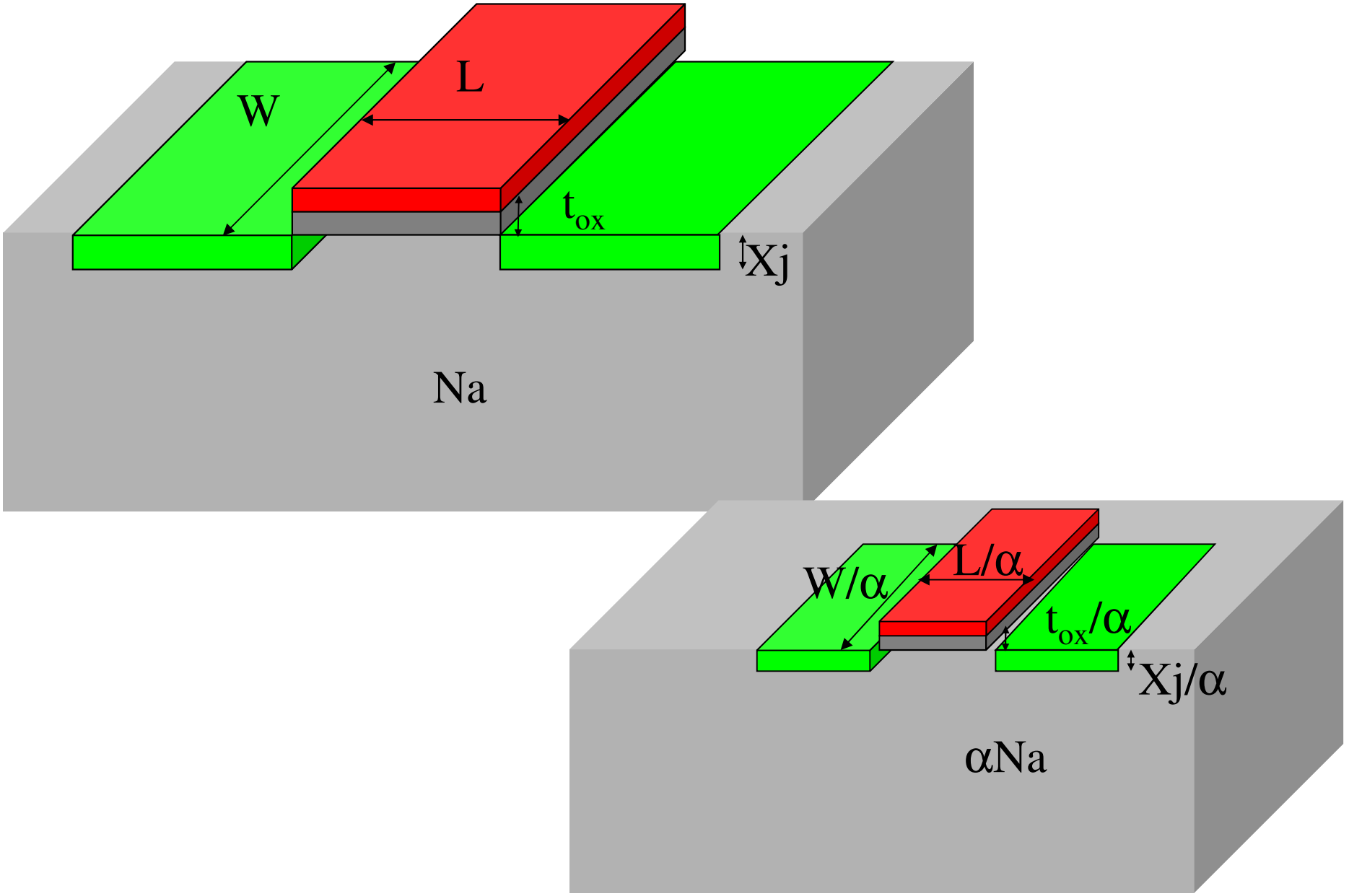
Layout of a circuit of inverter and NOR

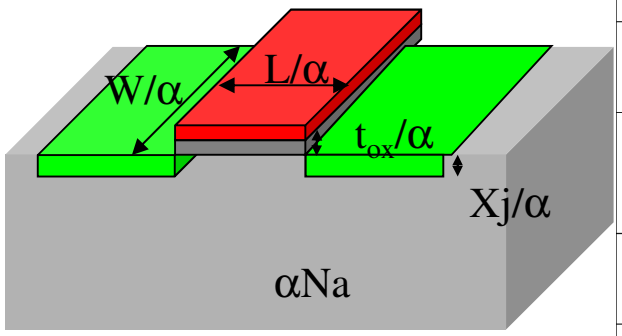


Block Layout



Scaling of processes by a factor α





Scaling with constant	Voltage	Field
Channel length L	1/α	1/α
Channel width W	1/α	1/α
Area A=W * L	$1/\alpha^2$	$1/\alpha^2$
Oxide thickness tox	1/α	1/α
Power supply U_{DD}	1	1/α
Beta $\beta=\mu(W/L)(\varepsilon_{ox}/t_{ox})$	α	α
Current $I=\frac{1}{2}\beta(U_{GS}-U_T)^2$	α	1/α
Gate capacity $W*L*\varepsilon_{ox}/t_{ox}$	1/α	1/α
Delay time $t_{f,r}=4C_L/\beta*U_{DD}$	$1/\alpha^2$ (C_L/α)	1/α (C_L)
Clock rate f=1/T	α^2	α
Dyn. power loss $Pd=f*C_L*U_{DD}^2$	α	$1/\alpha^2$
Current density J=I/A	α^3	α
Power density P/A	α^3	1

The elctrical field will be maintained constant

Example of modern CMOS processes

Technology	0.18um	0.15um	0.13um	90nm
Production Start	1Q99	1Q00	1Q01	3Q02
Core Vdd	1.5V-1.8V	1.2-1.5V	1.0-1.5V	1.0-1.2V
IO Vdd	2.5V, 3.3V	2.5V, 3.3V	2.5V, 3.3V	1.8V-3.3V
Poly Half-pitch	0.215um	0.185um	0.155um	0.12um
Gate Length(Physical)	0.16-0.13um	0.11-0.12um	0.08-0.085um	45-80nm
Gate Dielectric (EOT) - Core - I/O, Analog Option	 26A, 32A 50A, 70A	 20A, 26A 50A, 70A	 16-26A 50A, 70A	 13-22A 28A-70A
Metal Layers	6 Al	7 Al or Cu	7 - 8 Cu	9 - 10 Cu
BEOL Dielectric (k)	Low k (3.6)	Low-k (3.6)	Low-k (2.9, 3.6)	Low-k (2.9, <2.5)
Contacted M1 Pitch	0.46um	0.39um	0.34 um	0.24um
Contacted Mx Pitch	0.56um	0.48um	0.41 um	0.28um
Top Metal Pitch (std)	0.9um	0.9um	0.9 um	0.84um
Emb-6T SRAM Cell	4.65 um^2	3.42 um^2	2.43, 2.14 um^2	1.27 um^2
Design Rules/SPICE	Available	Available	Available	Available

Source: TSMC, 2003