Gates in CMOS-Technology

6. Standard/complex CMOS static logic gates

7. Special gates and their applications

- 7.1 Transmission gates
- 7.2 Clocked CMOS (Tri-state CMOS gates)
- 7.3 Bus-driver
- 7.4 Multiplexer

8. CMOS-circuit techniques (logic gates)

- 8.1 Pseudo-NMOS
- 8.2 Cascode-logic

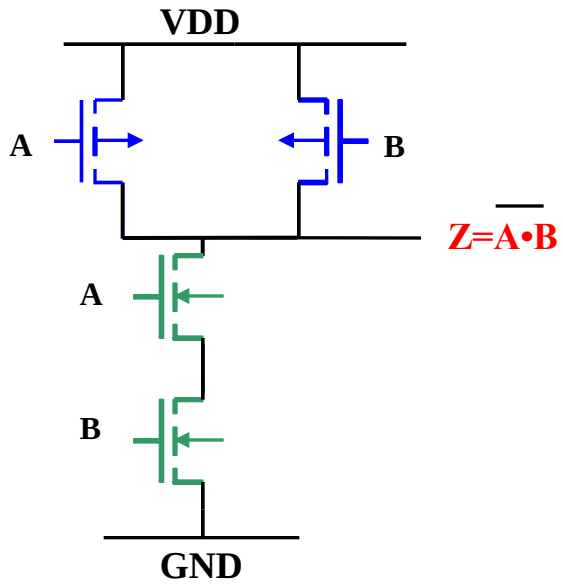
9. Dynamic logics (Precharge-Evaluate)

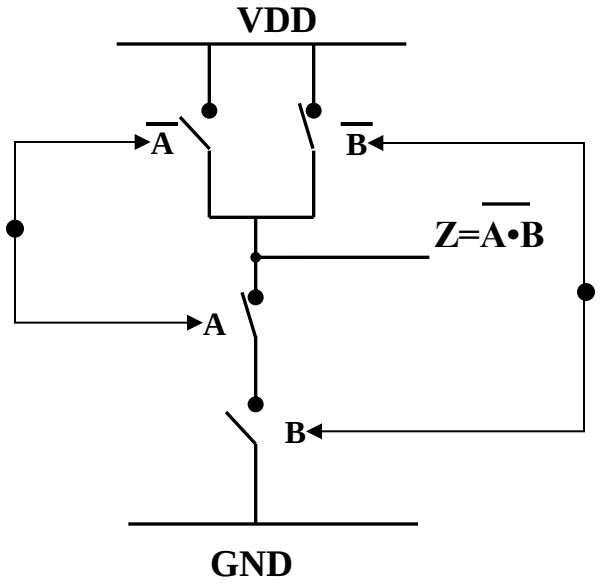
10. Summary:

CMOS-circuit types for combinatorial circuits

- 10.1 Advantages and disadvantages of static logics
- 10.2 Advantages and disadvantages of dynamic logics

Gates in CMOS-Technology





NAND-Gates in CMOS-Technology

A	Tna	Tpa	B	Tnb	Tpb	Z
A = 0	blocks	conducts	B = 0	blocks	conducts	1
A = 0	blocks	conducts	B = 1	conducts	blocks	1
A = 1	conducts	blocks	B = 0	blocks	conducts	1
A = 1	conducts	blocks	B = 1	conducts	blocks	0

Principle of CMOS-Logics

AND-Conjunction ⇨Series circuit

OR-Conjunction ⇨Parallel circuit

$Z = f(A, B...)$

Path to V_{SS} (GND) of NMOS: $Z_N = \overline{f(A, B...)}$

Path to V_{DD} of PMOS: $Z_P = f(\overline{A}, \overline{B}...)$

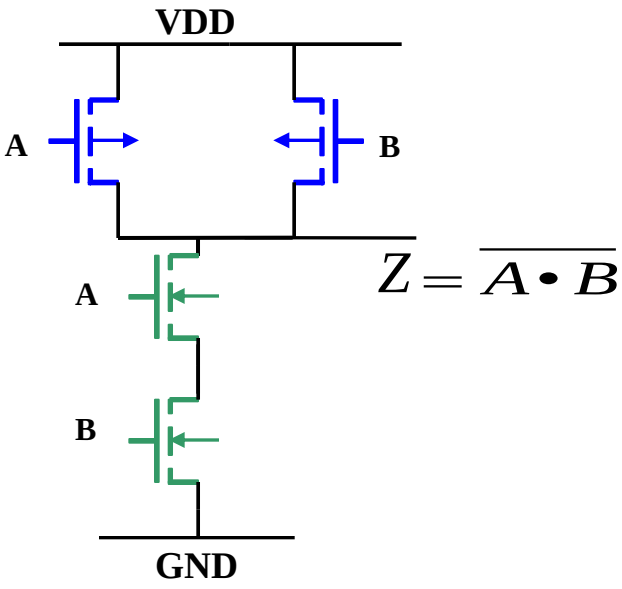
De Morgan Rules $Z = \overline{A \cdot B} = \overline{A} + \overline{B}$

$Z = \overline{A + B} = \overline{A} \cdot \overline{B}$

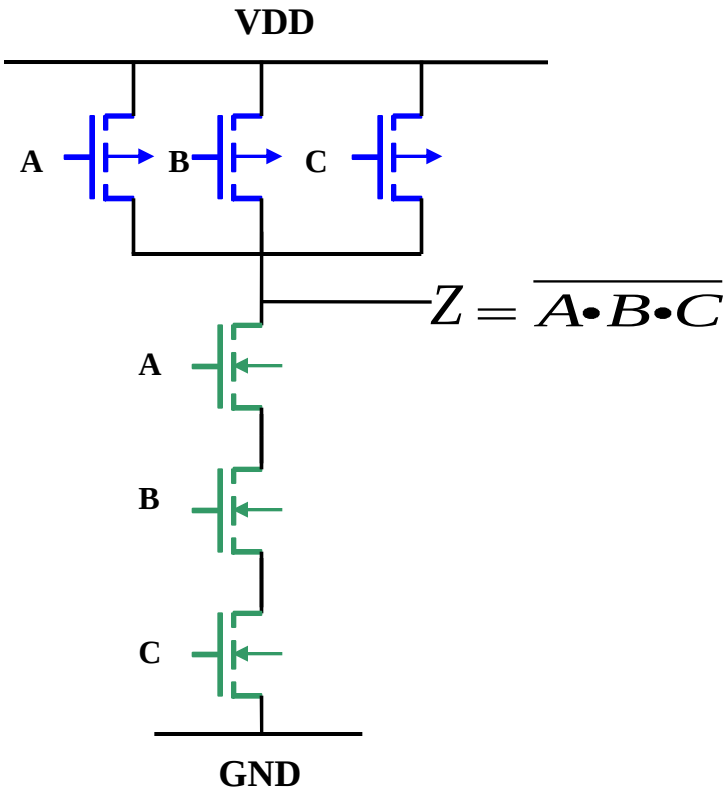
States of Transistors with NAND-Gates $\overline{A \bullet B}$

Path to V_{SS} (GND): $Z_N = \overline{Z} = A \bullet B$

Path to V_{DD}: $Z_P = Z = \overline{A \bullet B} = \overline{A} + \overline{B}$

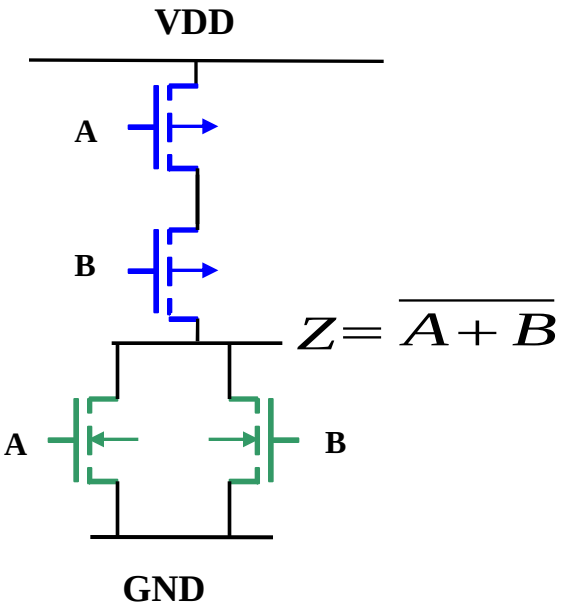


2-Input NAND

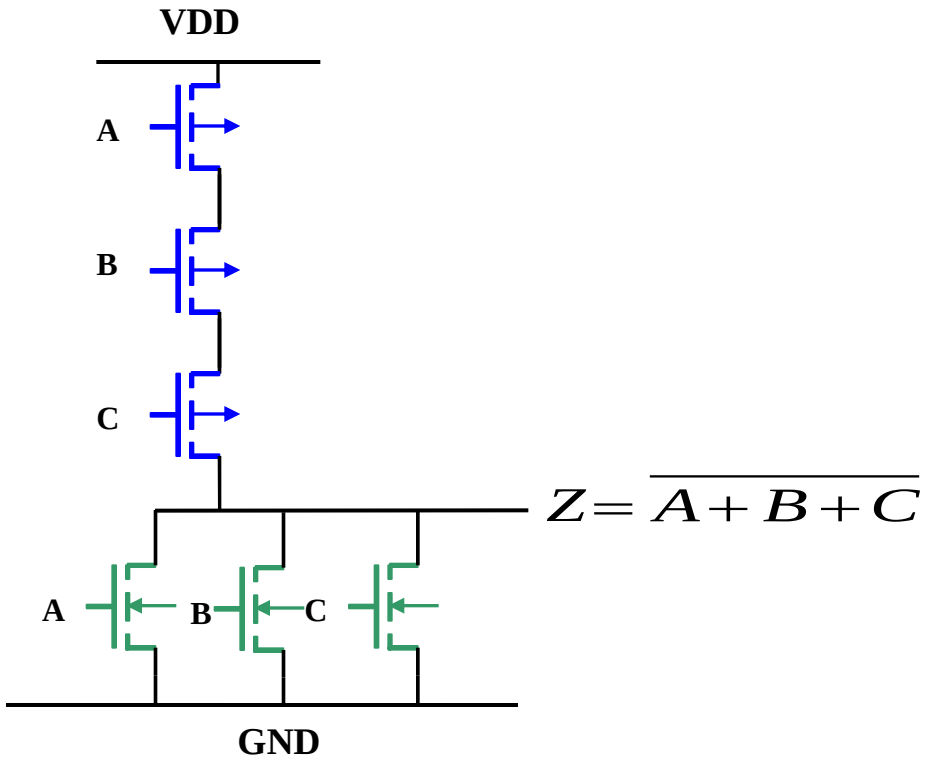


3-Input NAND

NOR Gates



2-Input NOR

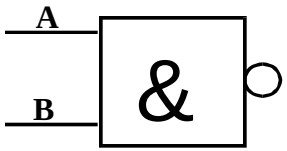


3-Input NOR

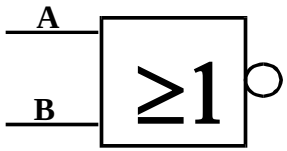
$$Z_N = \overline{Z} = A + B$$

$$\rightarrow Z_P = \overline{A + B} = \overline{A} \bullet \overline{B} = Z$$

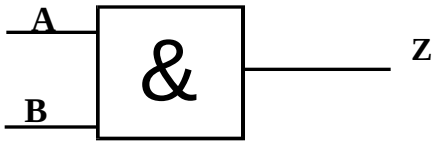
Only inverted functions directly realized



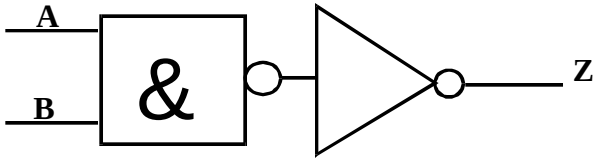
2-input NAND



2-input NOR

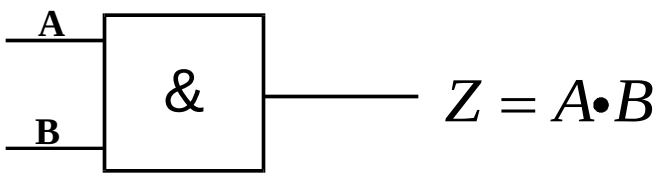


2-input AND

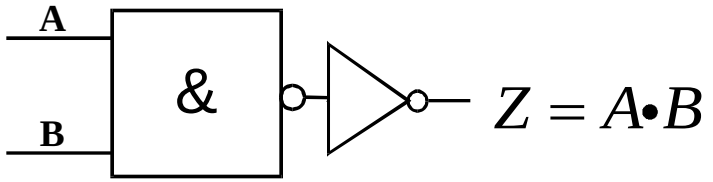


2-input AND

De Morgan Rules

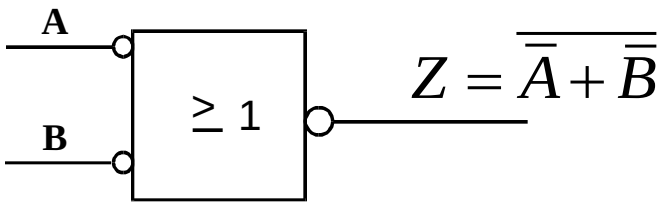


Logic function

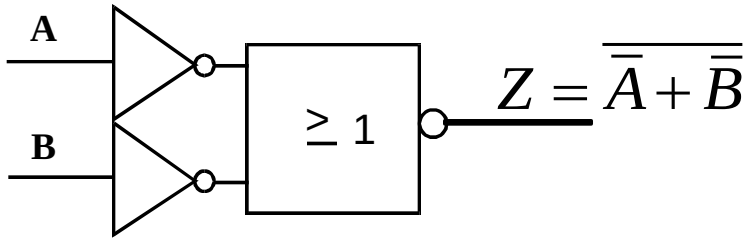


Realization

De Morgan: $Z = A \bullet B = \overline{\overline{A} + \overline{B}}$

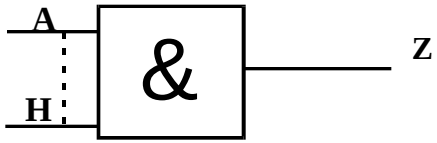


Logic function

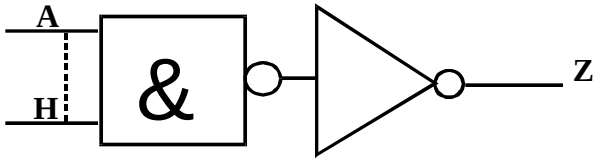


Alternative realization

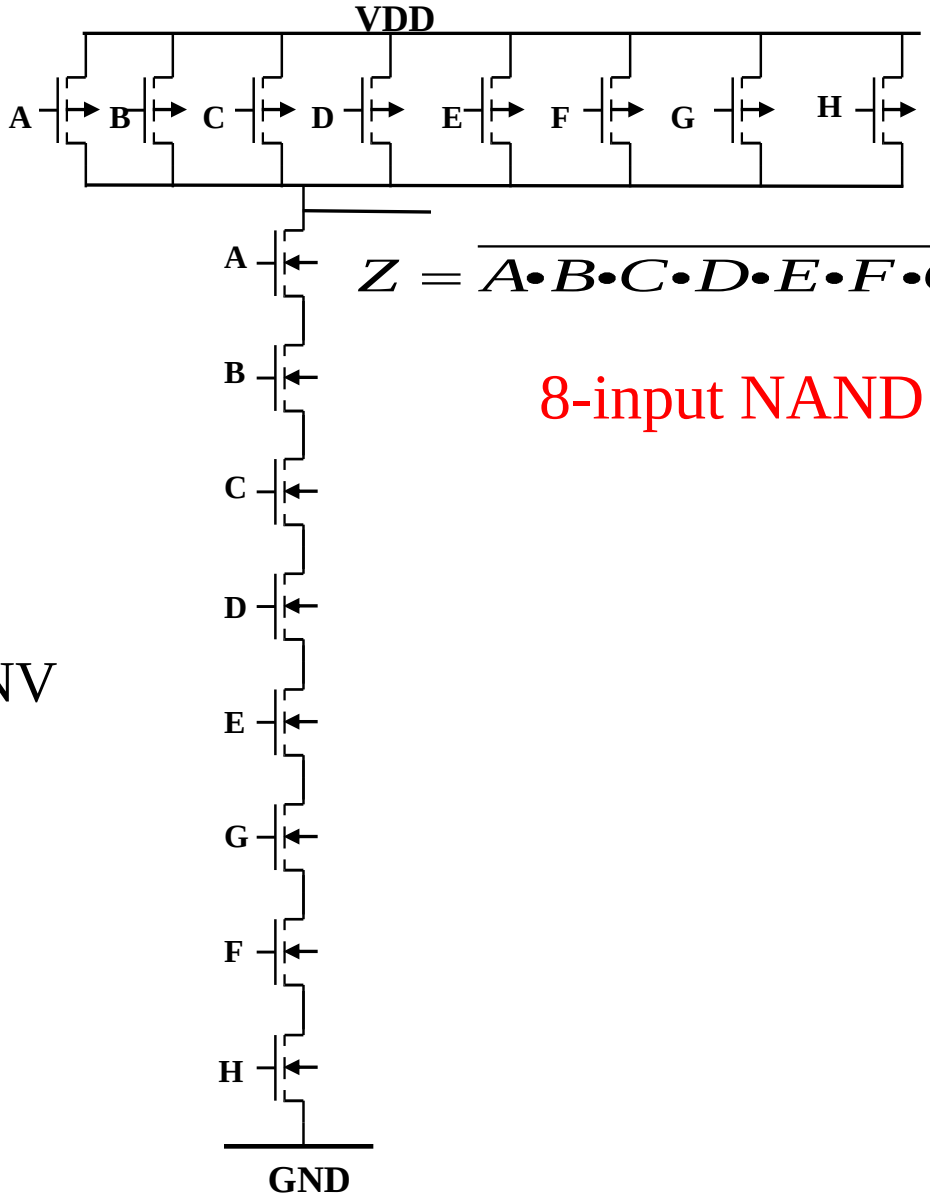
Realization of an 8-input AND



8-input AND



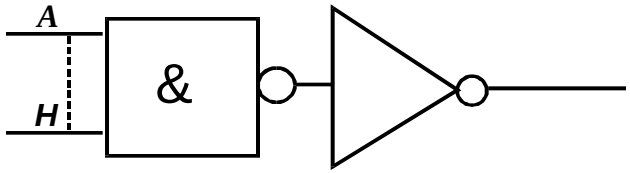
8-input AND = 8-fold NAND + INV



$$Z = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$$

8-input NAND

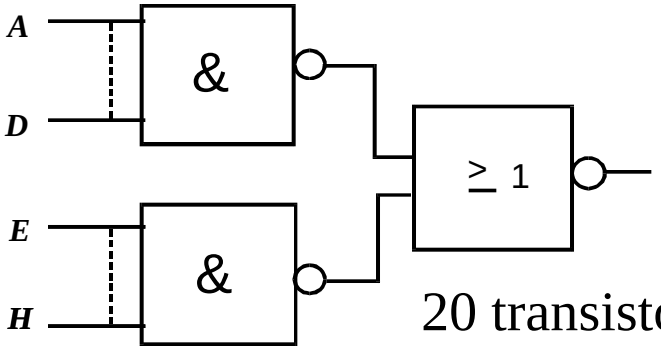
Alternative realization of a 8-input AND-function



18 transistors

$$Z = \overline{\overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}}$$

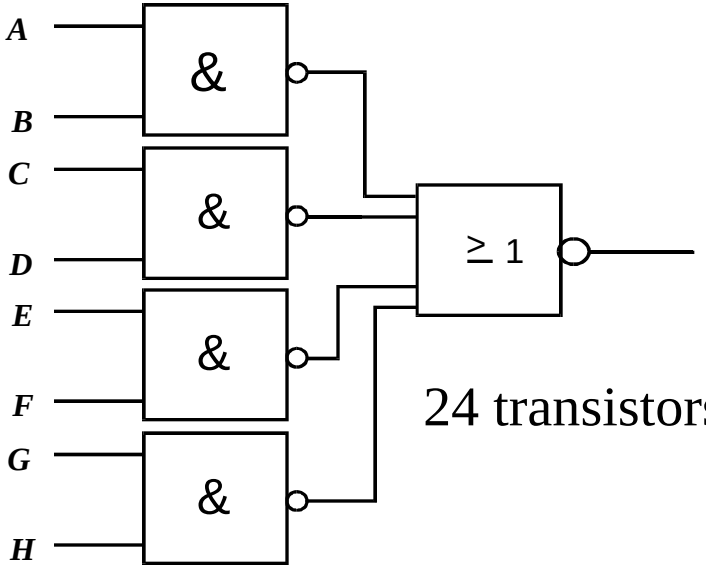
$t_d = 6.2\ ns$



20 transistors

$$Z = \overline{\overline{A \bullet B \bullet C \bullet D} + \overline{E \bullet F \bullet G \bullet H}}$$

$t_d = 5.2\ ns$

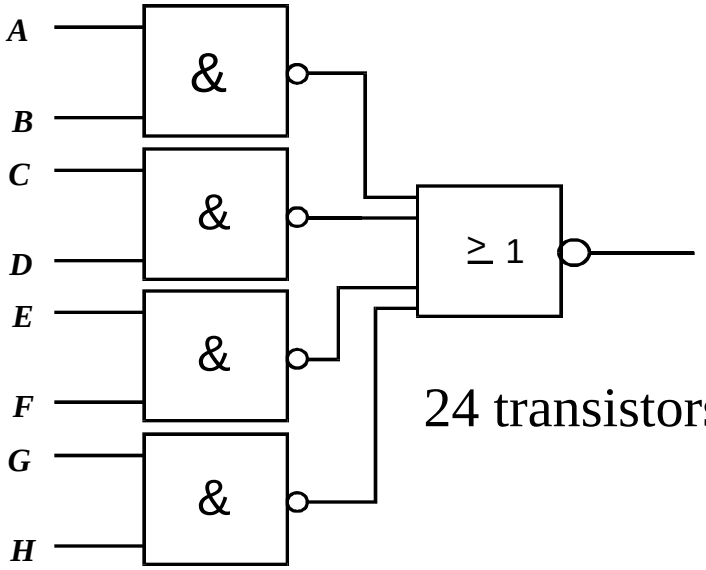


24 transistors

$$Z = \overline{\overline{A \bullet B} + \overline{C \bullet D} + \overline{E \bullet F} + \overline{G \bullet H}}$$

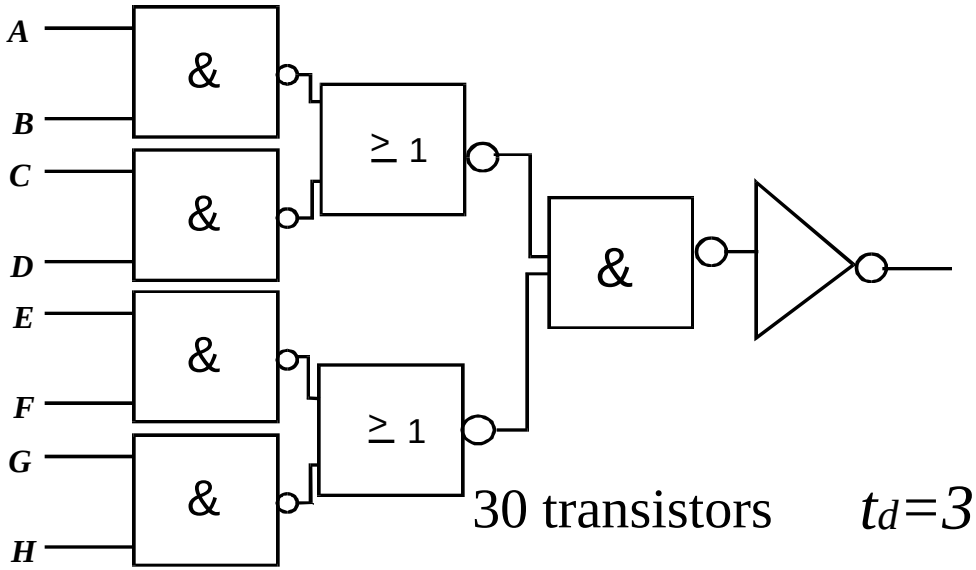
$t_d = 4.2\ ns$

Realization of a 8-fold AND-Gate



$$Z = \overline{\overline{A \bullet B} + \overline{C \bullet D} + \overline{E \bullet F} + \overline{G \bullet H}}$$

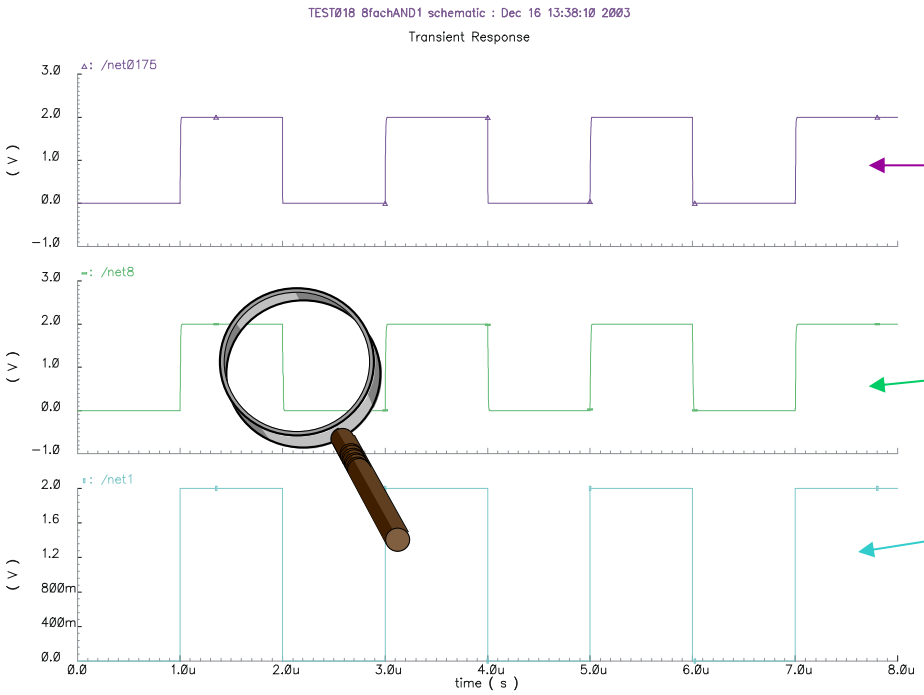
24 transistors $t_d = 4.2\ ns$



$$Z = \overline{\overline{\left(\overline{A \bullet B} + \overline{C \bullet D}\right) \bullet \left(\overline{E \bullet F} + \overline{G \bullet H}\right)}}$$

30 transistors $t_d = 3.2\ ns$

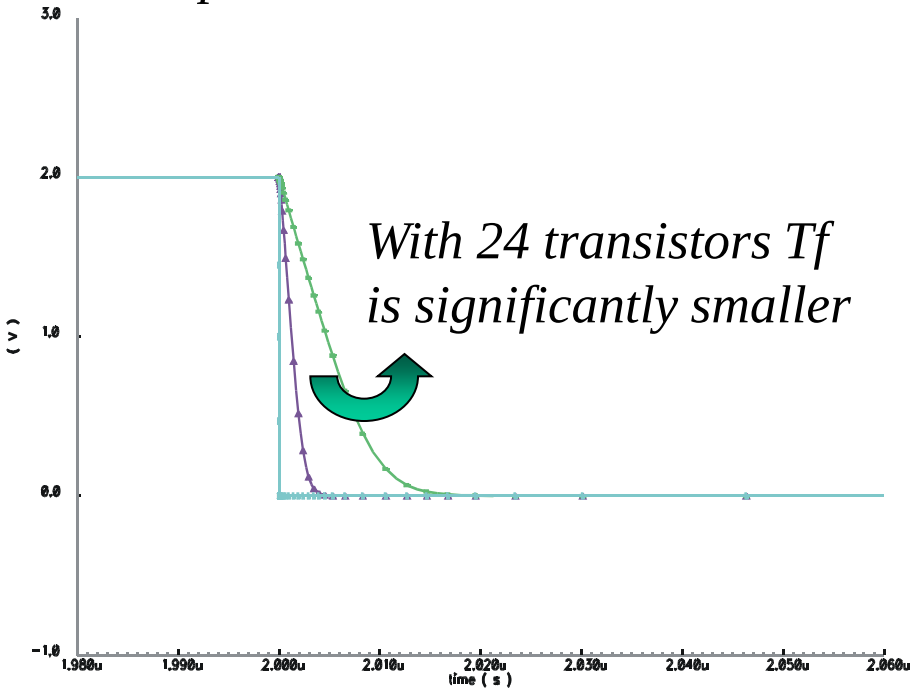
Analog Simulation & Analysis



Output Z with 24 transistors

Output Z with 18 transistors

Input A

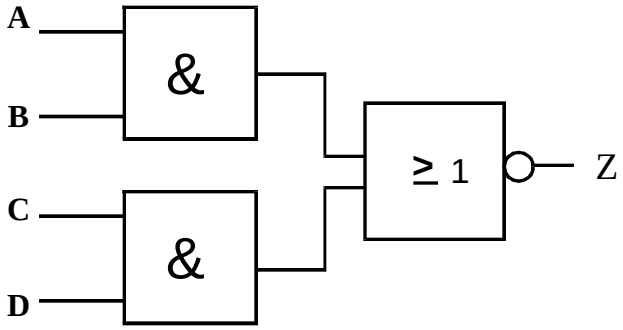


With 24 transistors Tf is significantly smaller

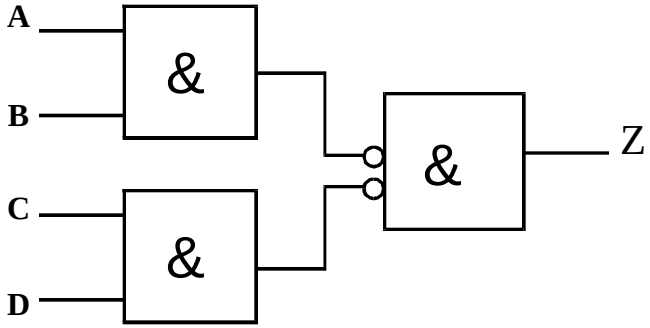
Complex gates:

$$Z = \overline{A \bullet B + C \bullet D}$$

16 transistors

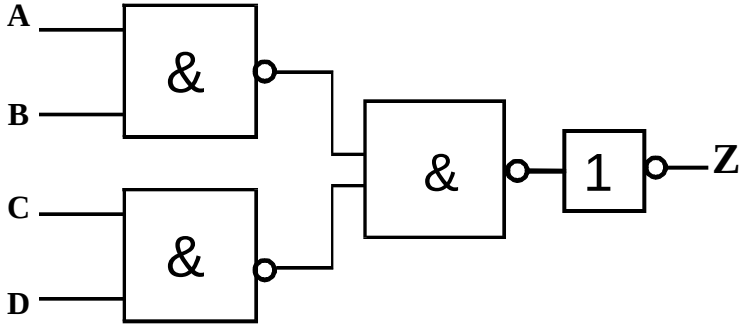


$$= \overline{\overline{A \bullet B} \bullet \overline{C \bullet D}}$$



$$= \overline{\overline{\overline{A \bullet B} \bullet \overline{C \bullet D}}}$$

14 transistors



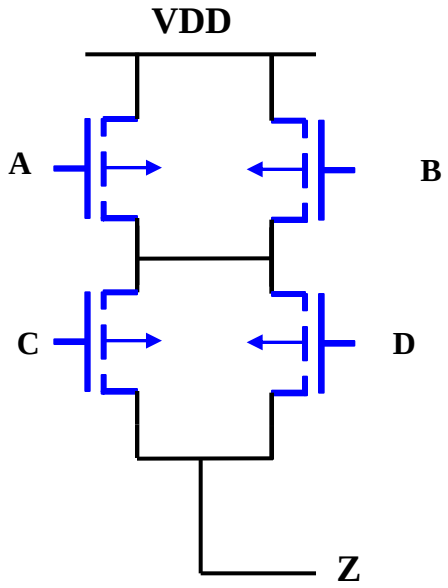
n- and p-parts of complex gate

$$Z_P = Z = \overline{A \bullet B + C \bullet D}$$

$$= \overline{A \bullet B} \bullet \overline{C \bullet D}$$

$$= \left(\bar{A} + \bar{B}\right) \bullet \left(\bar{C} + \bar{D}\right)$$

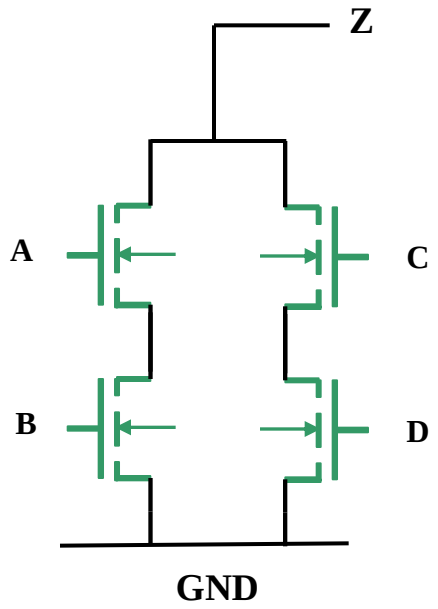
p-part



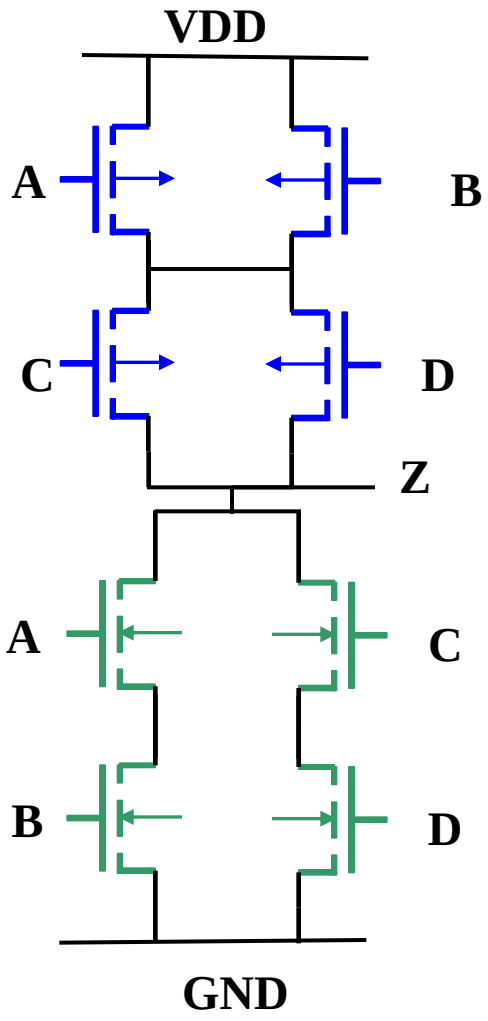
$$Z = \overline{A \bullet B + C \bullet D}$$

$$Z_n = \bar{Z} = A \bullet B + C \bullet D$$

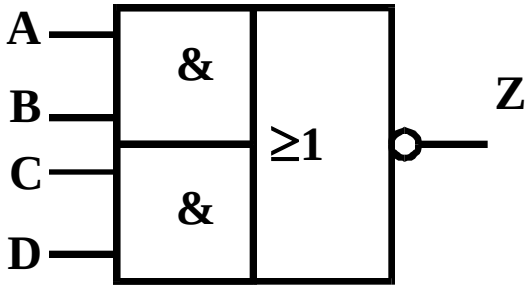
n-part



Complex gate and its symbol (1)

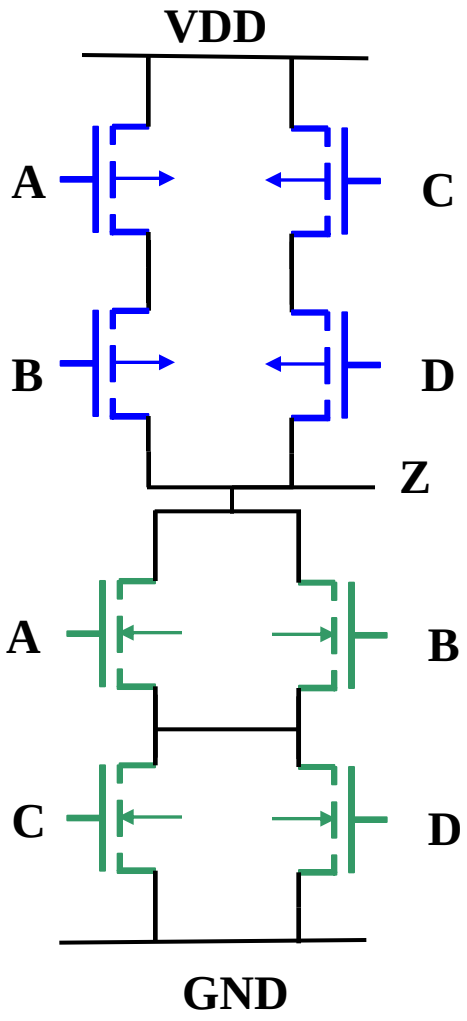


$$Z = \overline{A \bullet B + C \bullet D}$$

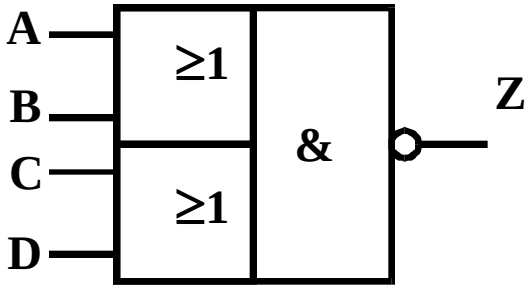


$A_{nd}\ O_{r}\ I_{nverter}$ - AOI-Gates

Complex gate and its symbol (2)



$$Z = \overline{(A+B)\cdot(C+D)}$$



$O_r A_{nd} I_{nverter}$ - OAI-Gates

CMOS static logic gates

=> Negative logics

=> For each input => 2 transistors

=> Series-/ parallel -circuits

=> Limited number of transistors connected in series

=> Preferably NANDs *(instead of NOR)*

=> Current path to V_{SS} (Zn) and V_{DD} (Zp) alternating

=> No static current consumption

Gates in CMOS-Technology

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   - 7.4 Multiplexer

8. CMOS-circuit techniques (logic gates)
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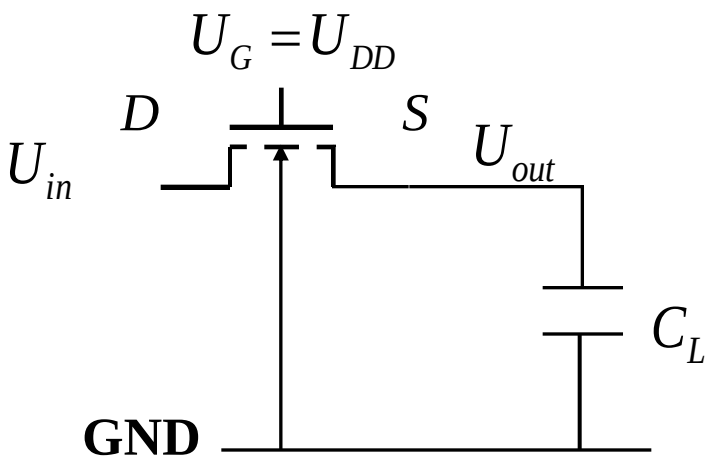
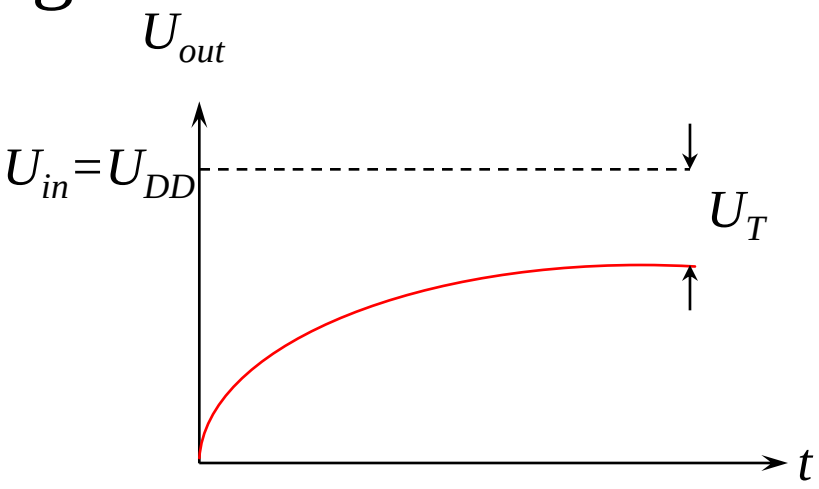
10. Summary:
    - CMOS-circuit types for combinatorial circuits
    - 10.1 Advantages and disadvantages of static logics
    - 10.2 Advantages and disadvantages of dynamic logics

Transmission gates





n-channel transmission gates

If $U_{in} = U_{out} \Rightarrow U_{DS} = 0 \Rightarrow I_D = 0$

Assumed initial state:

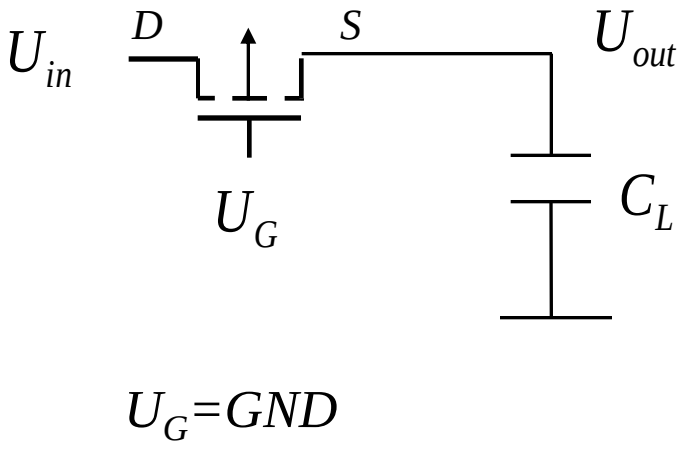
$U_G = U_{DD}$, $U_{out} = U_S = 0$, $U_{in} = U_D = 0 \nearrow U_{DD}$

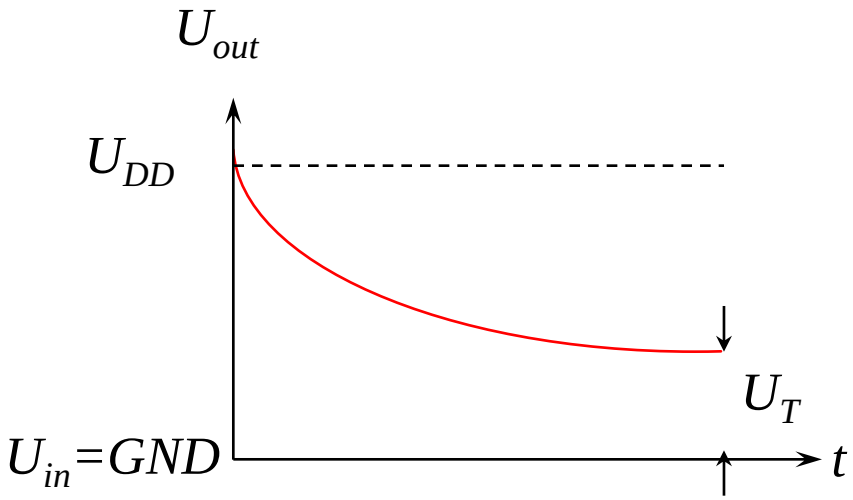
C_L is charged until: $U_{GS} = U_T \Rightarrow I_D = 0$

Then $U_{out} = U_{DD} - U_T$

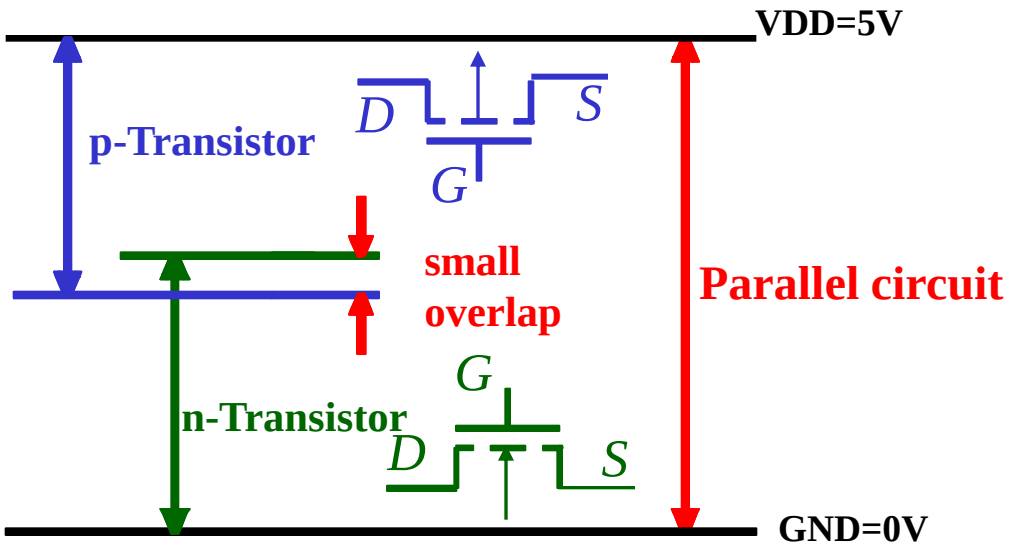
Wherein $U_T = U_{T0} + \gamma\left(\sqrt{U_{SB} + 2\phi_D} - \sqrt{2\phi_D}\right)$

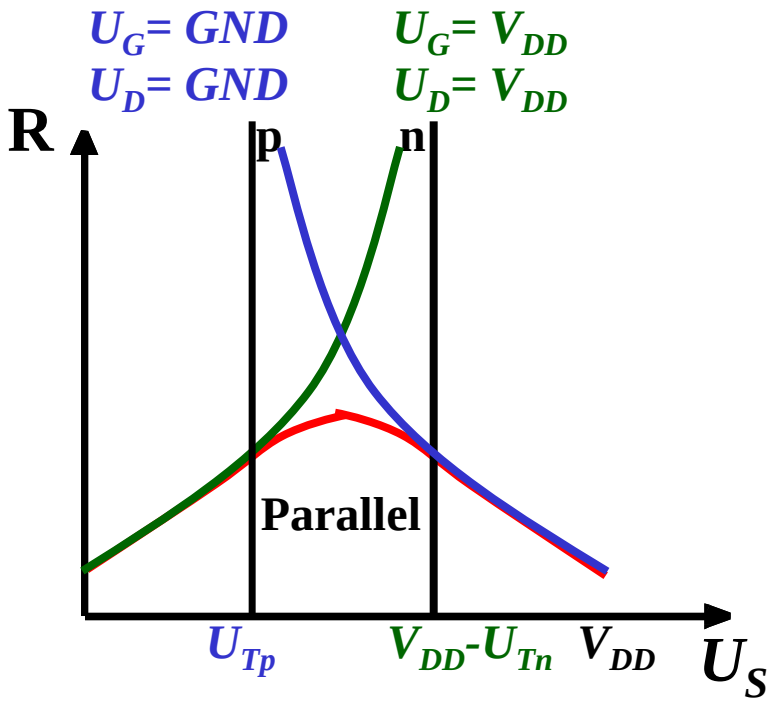
p-channel transmission gates

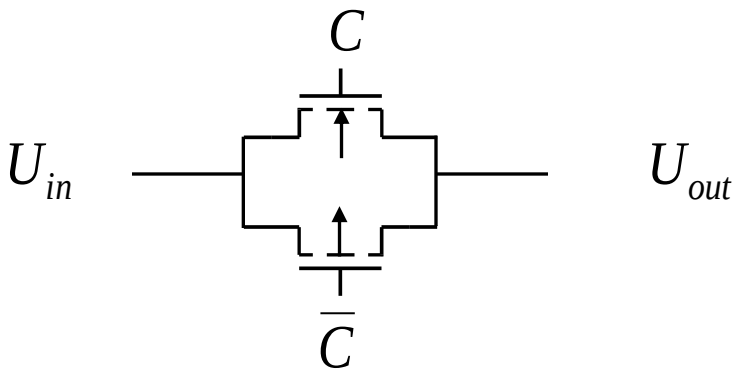




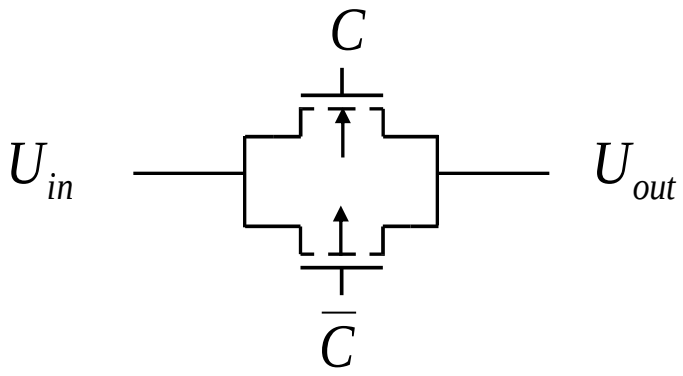
Voltage ranges and resistance of CMOS-transmission gates



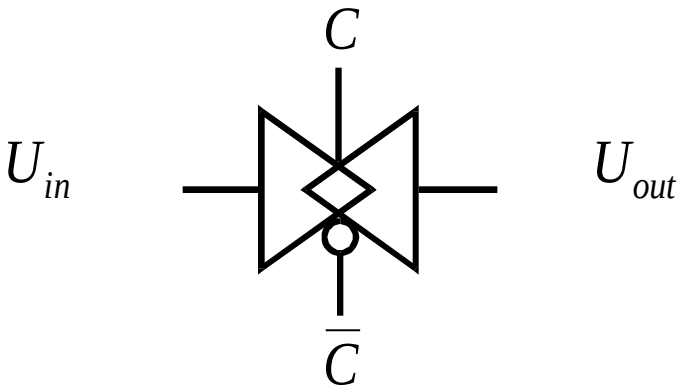




Behaviour of CMOS-Transmission Gate

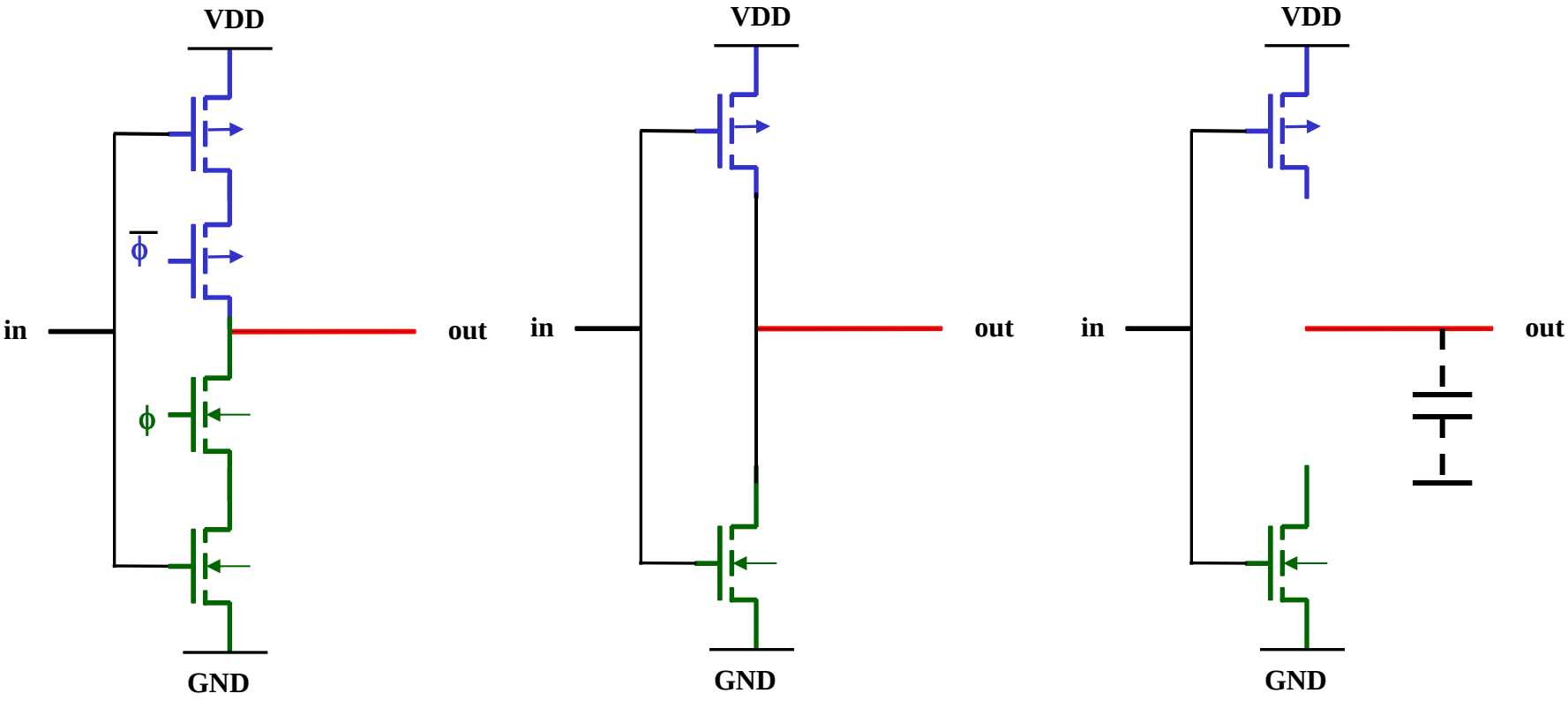


C	$T_N(C)$	$T_P(\overline{C})$	out
0	blocks	blocks	High-impedance
1	conducts	condcuts	out = in



CMOS-Transmission-Gate Symbol

Clocked CMOS Inverter



C^2MOS-Inverter

Also called:
Gated Inverter,
Tri-State Inverter

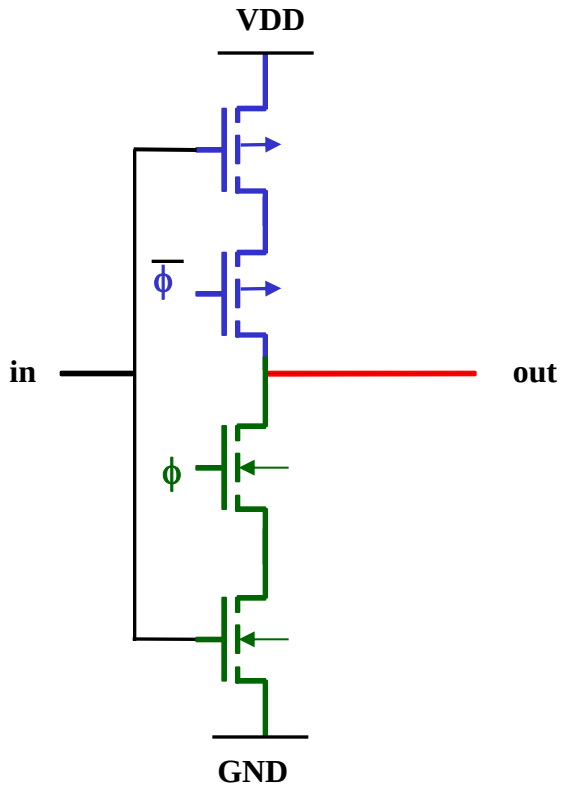
Tri-State Inverter $\Phi=1$

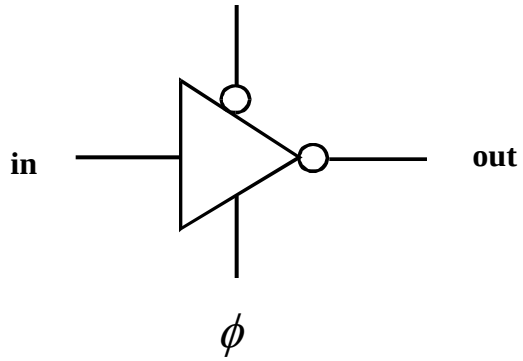
Normal inverter-function
in = 0 $\Rightarrow$ out = 1
in = 1 $\Rightarrow$ out = 0

Tri-State Inverter $\Phi=0$

out = high-impedance
State: Z

Tri-State CMOS Inverter

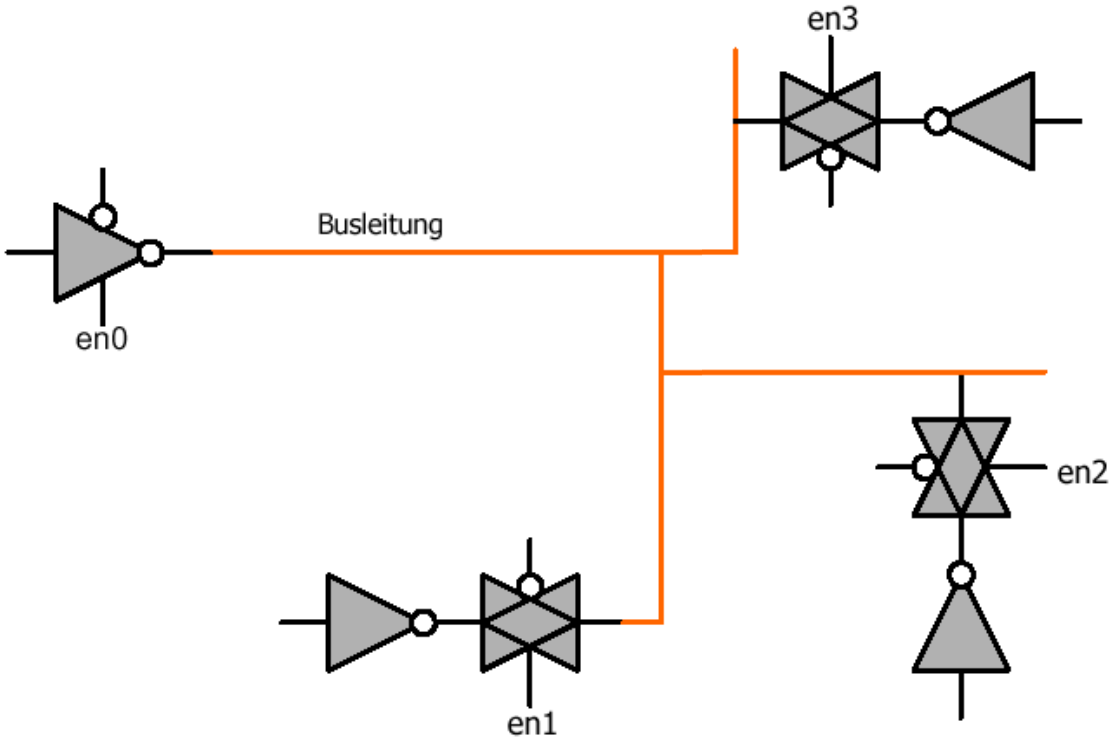




Applications: Dynamic switching (no short circuit)
Busse
Multiplexer
Latch

Driver for Busse

Bus is an effective method for exchanging information (data, instructions) between many units.



Simple driver:
Transmission Gate,
Gated Inverter

Important: the drivers must be controlled (en0, en1 ..) that way that only one signal is active, never several at the same time (transmission/write operation).

Passive: Output of driver is high-impedance / Tristate

Realization of multiplexer

Multiplexer function: $Out = SEL \cdot IN1 + \overline{SEL} \cdot IN2$

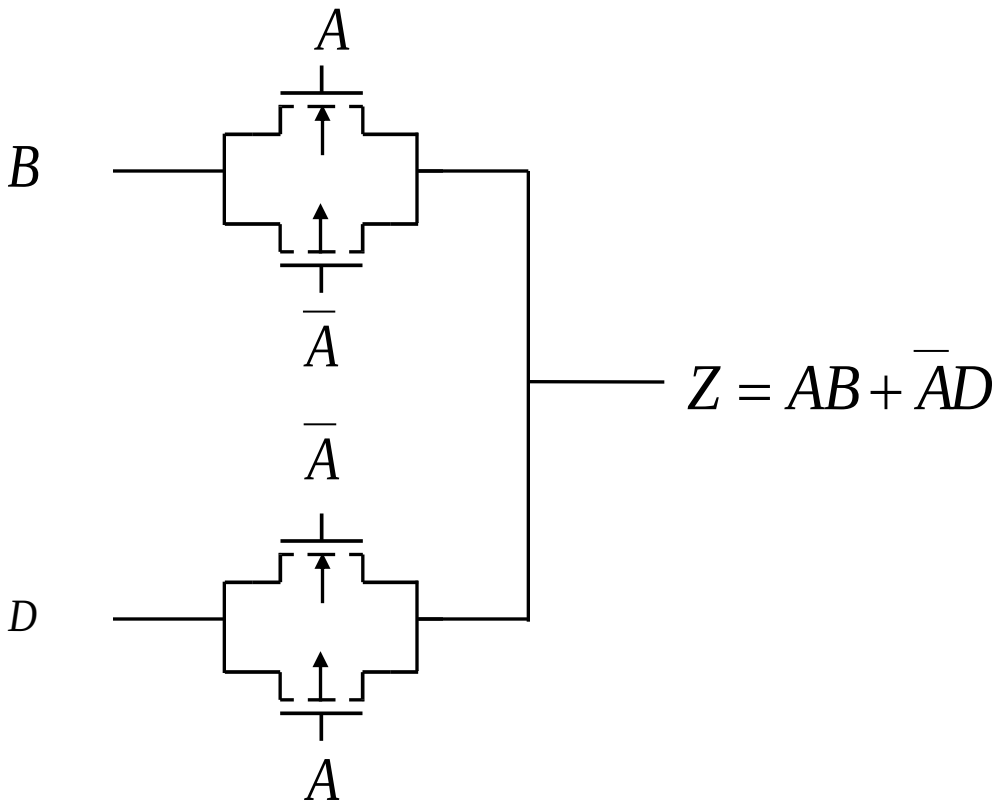
With SEL – Signal, one signal is chosen out of several inputs

SEL = 1 ⇨ Out = IN1
SEL = 0 ⇨ Out = IN2

A=1 ⇒ Z=B

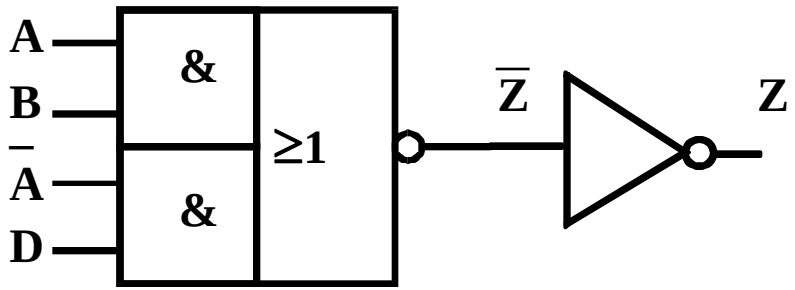
A=0 ⇒ Z=D

Realization with transmission gate



Multiplexer of AOI and OAI

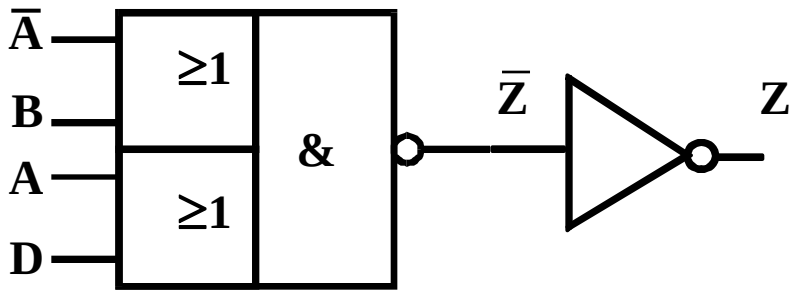
$$Z = \overline{\overline{A \bullet B + \overline{A} \bullet D}}$$



$$A = 1 \Rightarrow Z = B$$

$$A = 0 \Rightarrow Z = D$$

$$Z = \overline{\overline{(\overline{A} + B) \bullet (A + D)}}$$

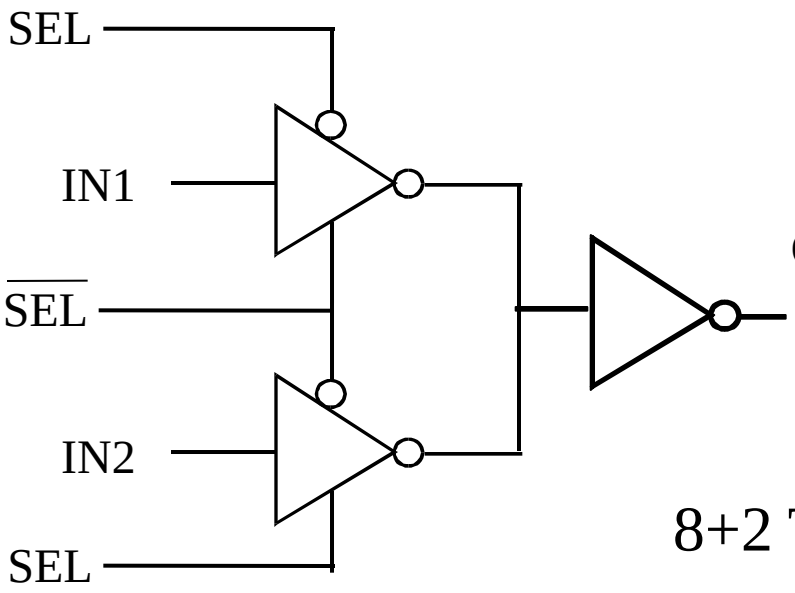


$$A = 1 \Rightarrow Z = B$$

$$A = 0 \Rightarrow Z = D$$

Complex-Gate: 8+2 transistors

Multiplexer of C^{2}MOS



SEL = 1 ⇨ Out = IN1
SEL = 0 ⇨ Out = IN2

8+2 Transistors

Comparison of multiplexer circuits

1) with transmission gate

\+ 4 transistors,

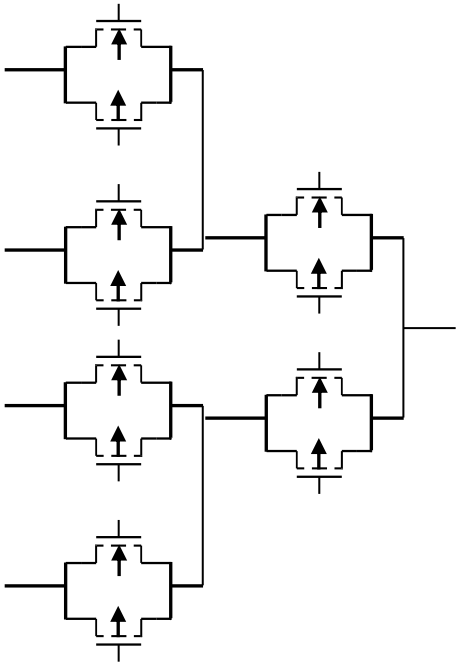
\- bad output (no signal regeneration)
especially with multi-stage multiplexer

2) with C^2MOS

8 + 2 transistors, 2 throughput times

3) with AOI or OAI:

8 + 2 transistors, 2 throughput times



Gates in CMOS-Technology

6. Standard/complex CMOS static logic gates

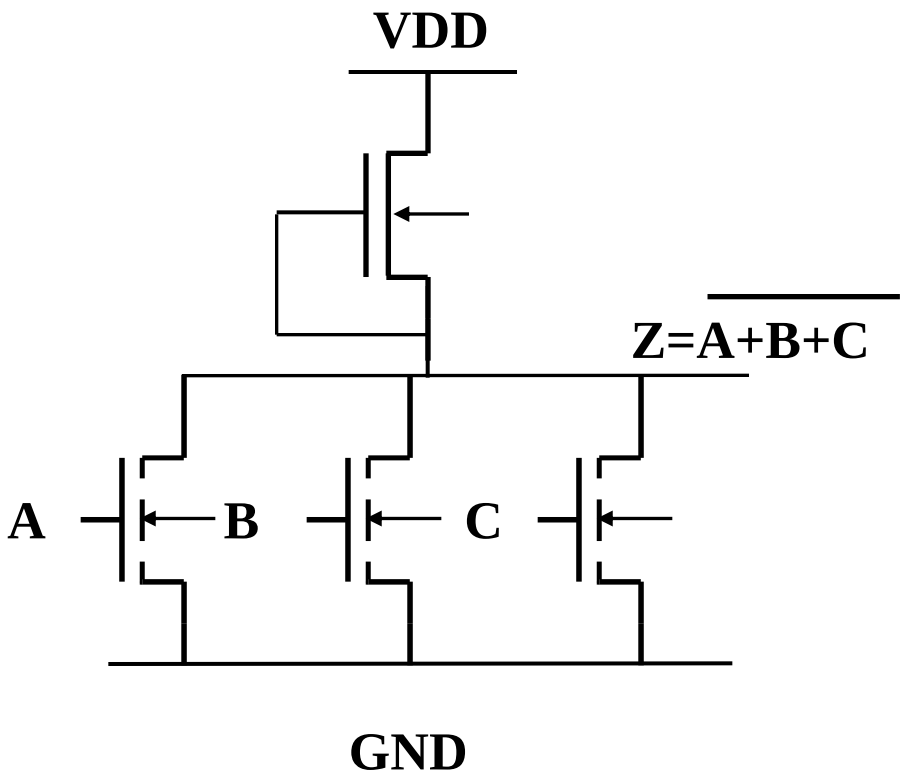
7. Special gates and the applications
    - 7.1 Transmission gates
    - 7.2 Clocked CMOS (Tri-state CMOS gates)
    - 7.3 Bus-driver
    - 7.4 Multiplexer

8. CMOS-circuit techniques (logic gates)
    - 8.1 Pseudo-NMOS
    - 8.2 Cascode-logic

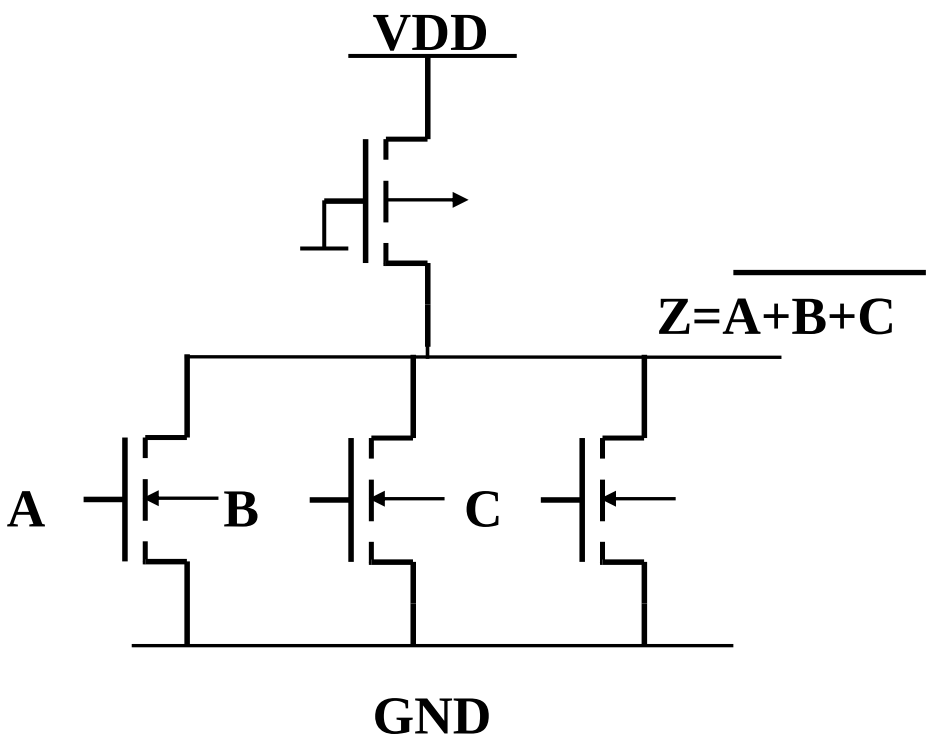
9. Dynamic logics (Precharge-Evaluate)

10. Summary:
    - CMOS-circuit types for combinatorial circuits
        - 10.1 Advantages and disadvantages of static logics
        - 10.2 Advantages and disadvantages of dynamic logics

Logic-Gates

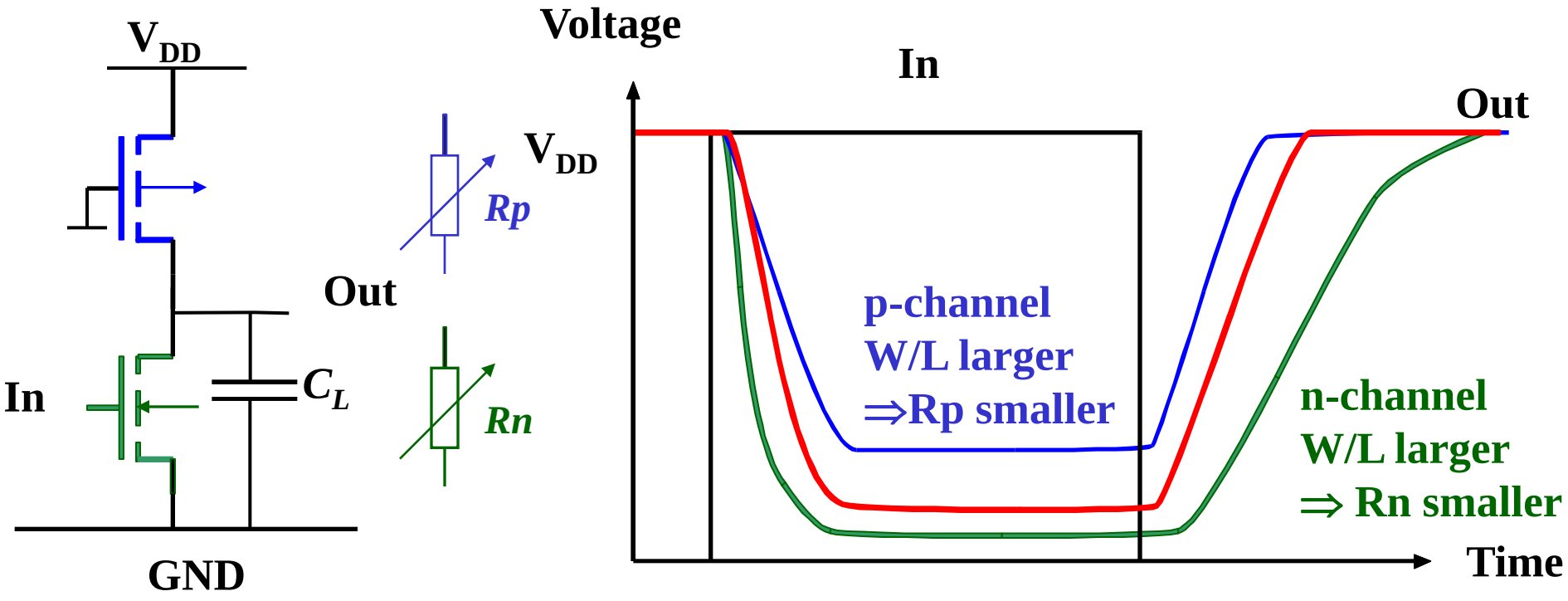


Enhancement/Depletion-NMOS



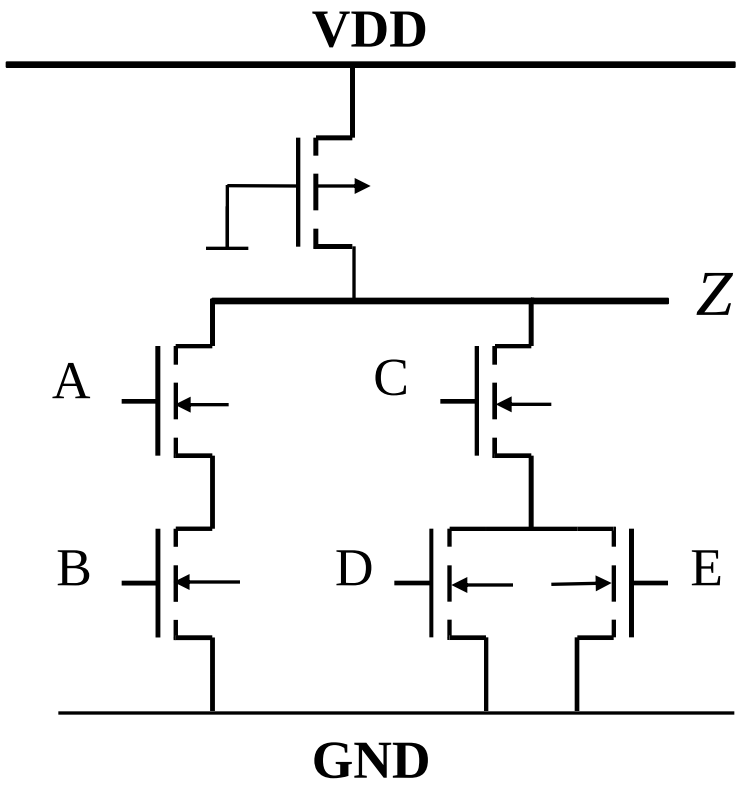
Pseudo-NMOS

Transfer curve of Pseudo-NMOS-Inverter



Careful dimensioning required.

Pseudo-NMOS Circuit technology



$$Z = \overline{A \bullet B + C \bullet (D + E)}$$

Advantages:

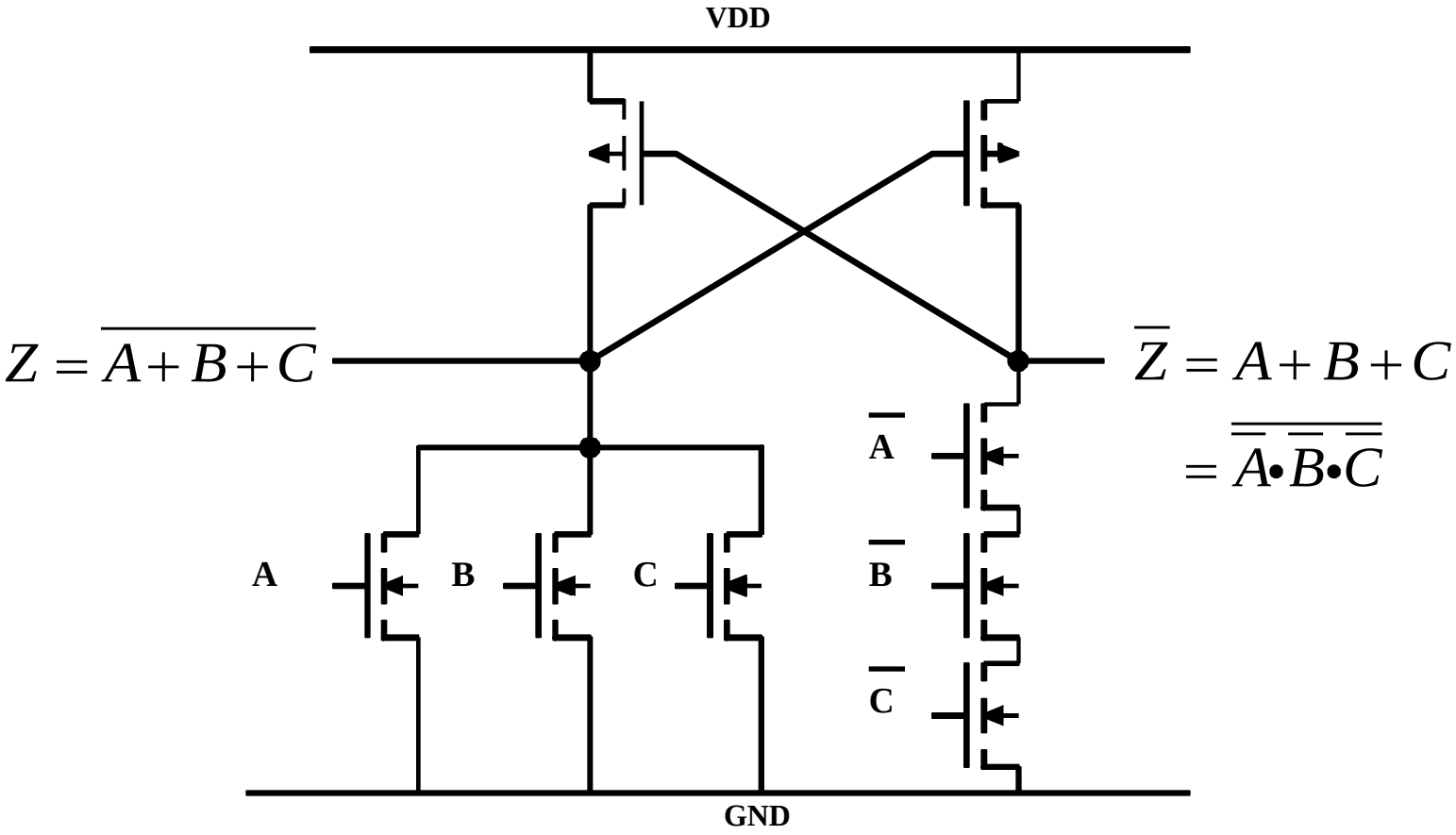
- Small area requirement (only 1 p-channel)
- Low capacitive load (only 1 transistor / input)
  - ➢ faster
  - ➢ low dynamic power loss

Disadvantage:

- High static power loss (if output is low)

Application: e.g. memory address-decoder: Z=(A1• A2• ... • A16)

Cascode-Logic



3-input NOR/OR in Cascode-Logic

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