# 11. Sequential Circuits

1. Realization of Registers
   (Latches, Flip-Flops)
   1. Dynamic Registers
   2. Static Registers
2. Pipeline
3. **Clock distribution – Clock networks**
4. **Clock generation**

# The role of the Clock- Network

Most widely spread network

Extremely high Fan-Out

Highest switching frequency

Significant share of power loss

Signal propagation in the clock network must be very fast

Signal propagation in the clock network must be very uniform (Skew!)

# Summary of Delay

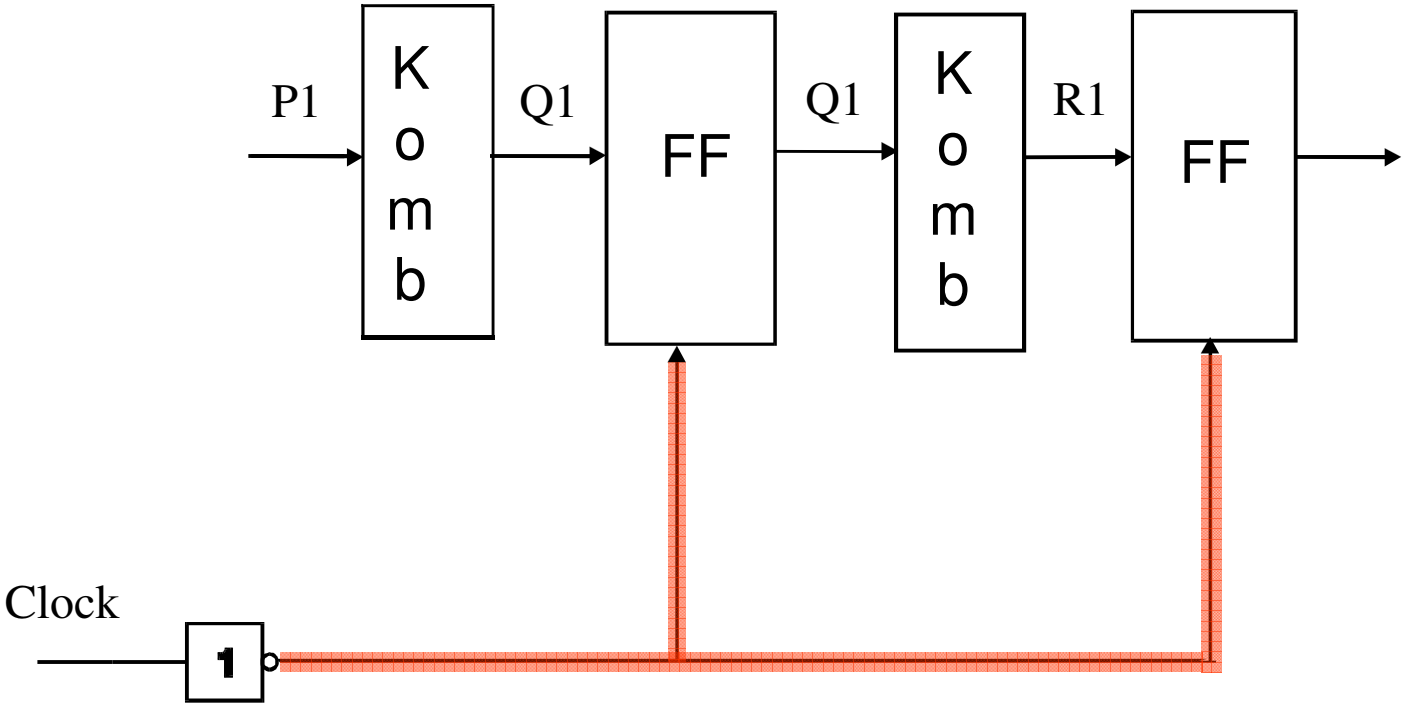
## Gate Delay

- Delay through a logic element
- independent of routing
- relatively predictable

## Interconnect Delay

- Signal delay through the wires
- strongly depending on routing
- difficult to predict

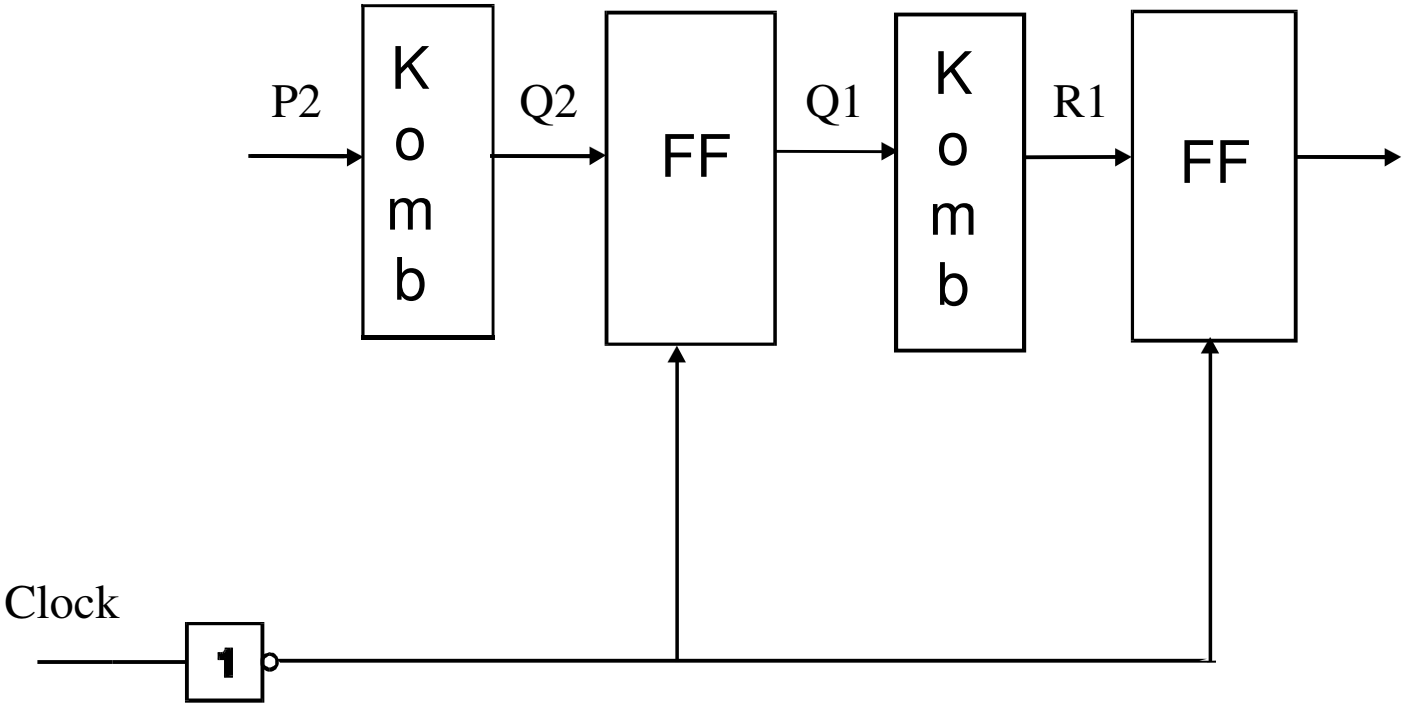
# Clock- / Driver




Data P1 Q1

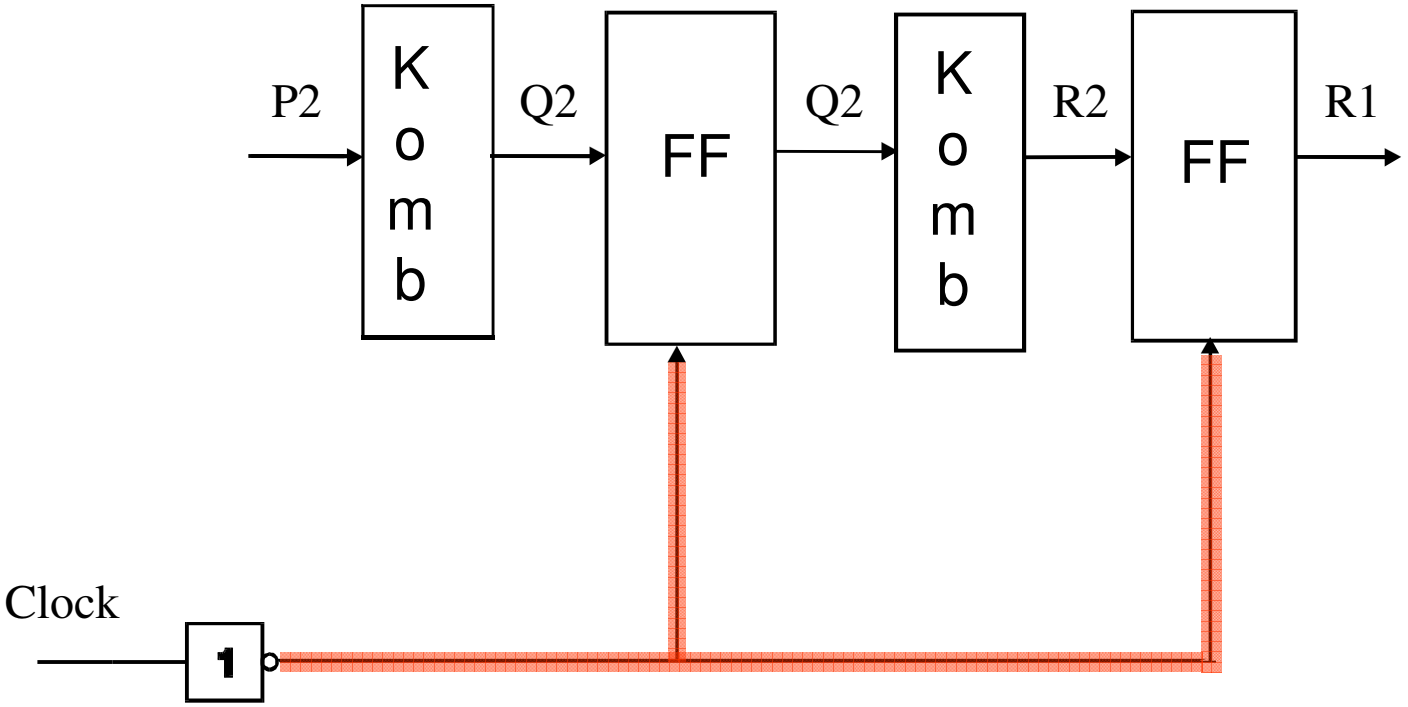
Clock P1 Q1 Q1 R1

# Clock- / Driver



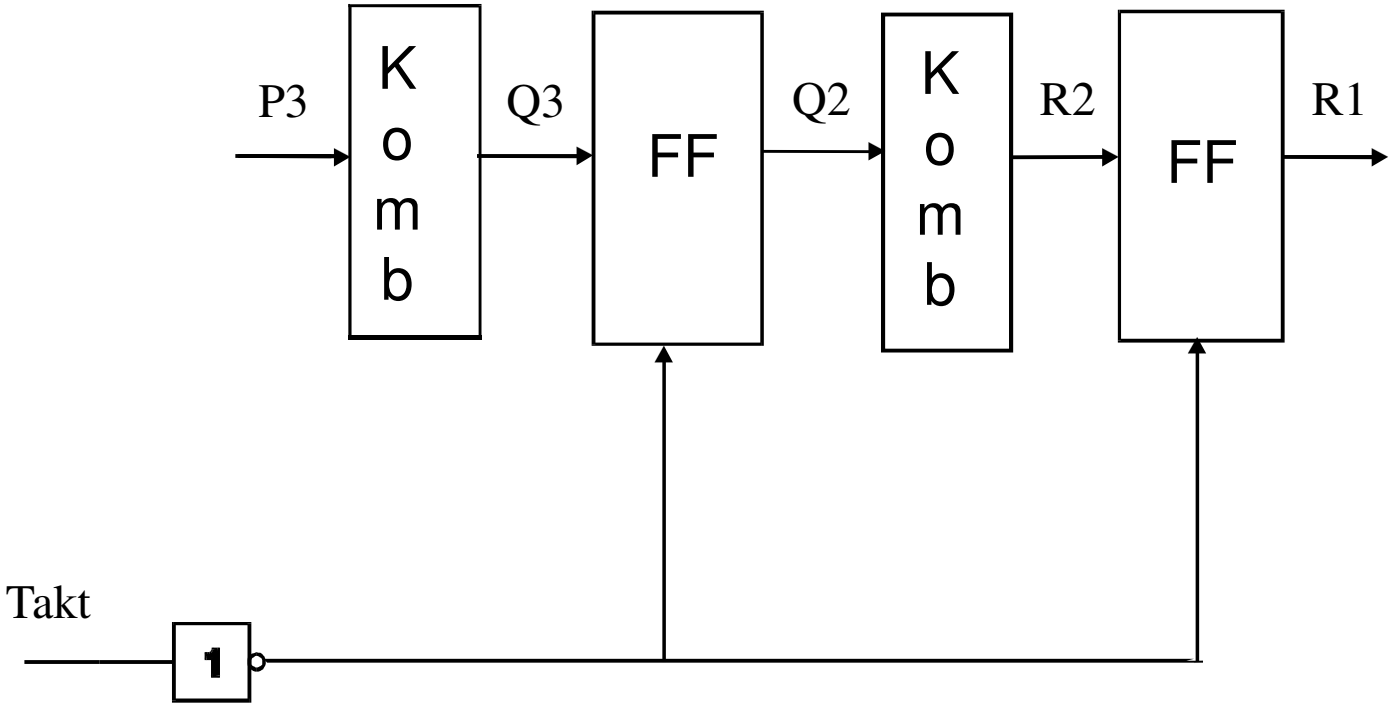

| | | | | |
|---|---|---|---|---|
| Data | P1 | Q1 | | |
| Clock | P1 | Q1 | Q1 | R1 |
| Data | P2 | Q2 | Q1 | R1 |

# Clock- / Driver



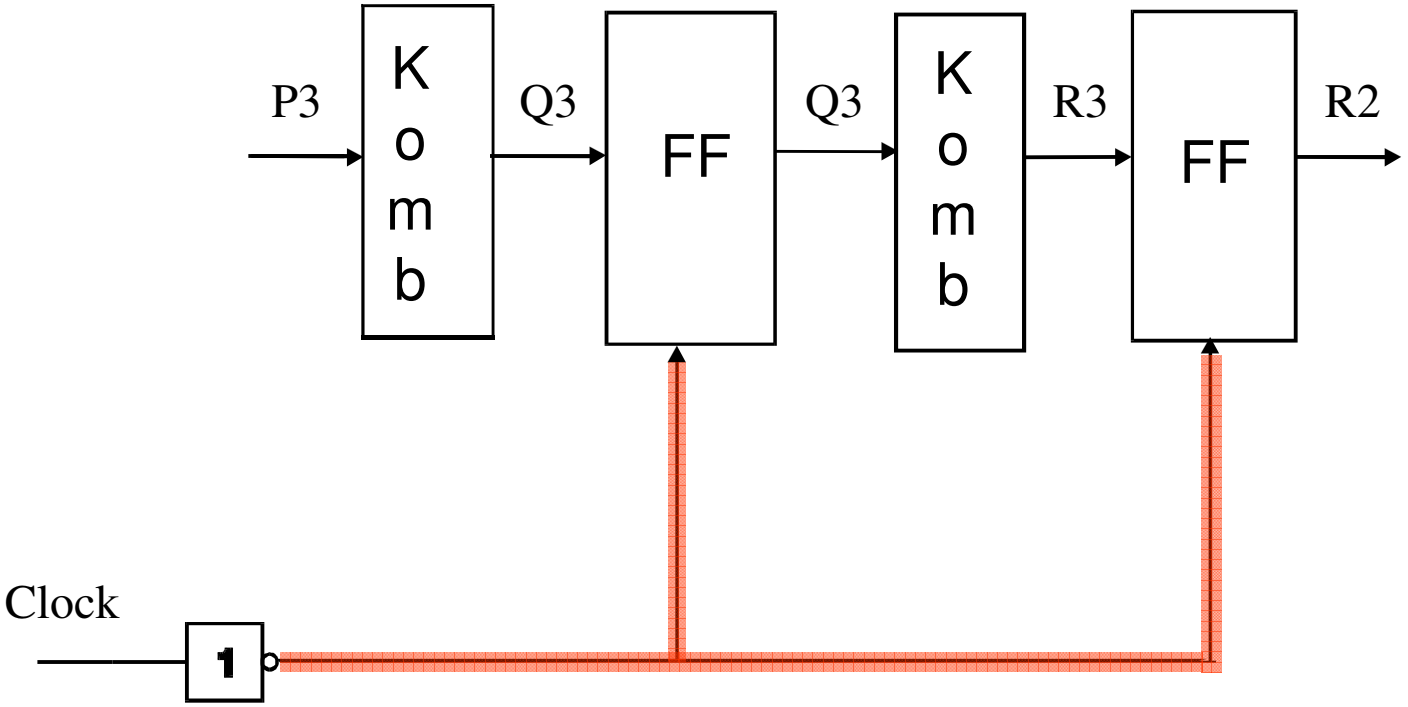

Data P1 Q1
Clock P1 Q1 Q1 R1
Data P2 Q2 Q1 R1
Clock P2 Q2 Q2 R2 R1

# Clock- / Driver



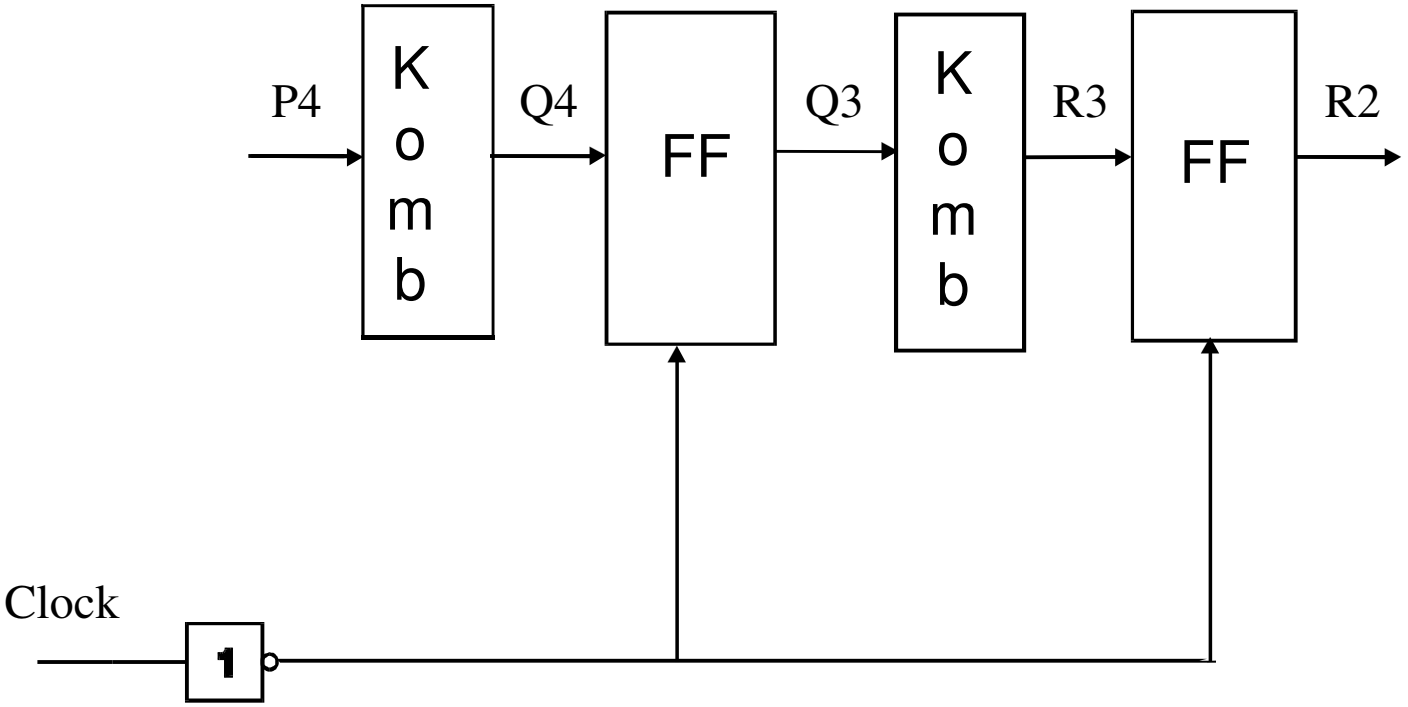

| | | | | | |
|---|---|---|---|---|---|
| Data | P1 | Q1 | | | |
| Clock | P1 | Q1 | Q1 | R1 | |
| Data | P2 | Q2 | Q1 | R1 | |
| Clock | P2 | Q2 | Q2 | R2 | R1 |
| Data | P3 | Q3 | Q2 | R2 | R1 |

# Clock- / Driver



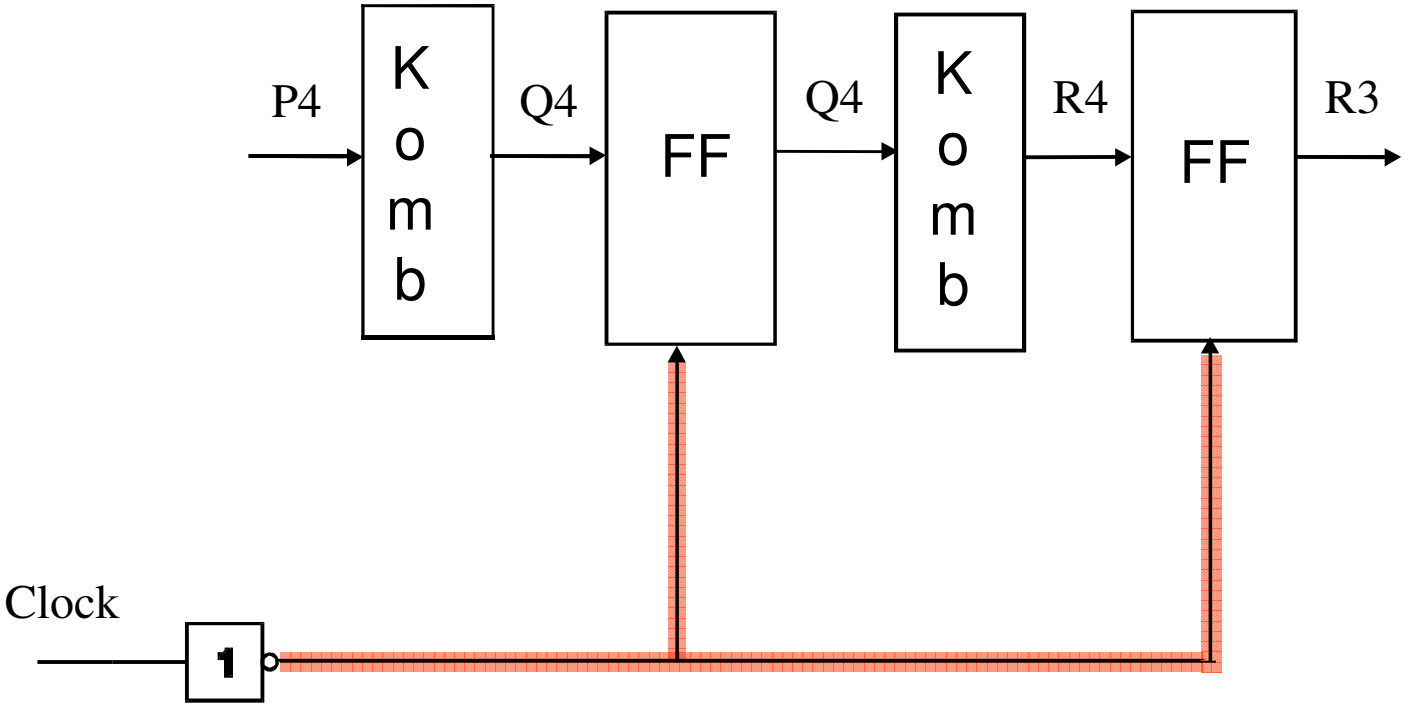

| | | | | | |
|---|---|---|---|---|---|
| Data | P1 | Q1 | | | |
| Clock | P1 | Q1 | Q1 | R1 | |
| Data | P2 | Q2 | Q1 | R1 | |
| Clock | P2 | Q2 | Q2 | R2 | R1 |
| Data | P3 | Q3 | Q2 | R2 | R1 |
| Clock | P3 | Q3 | Q3 | R3 | R2 |

# Clock- / Driver



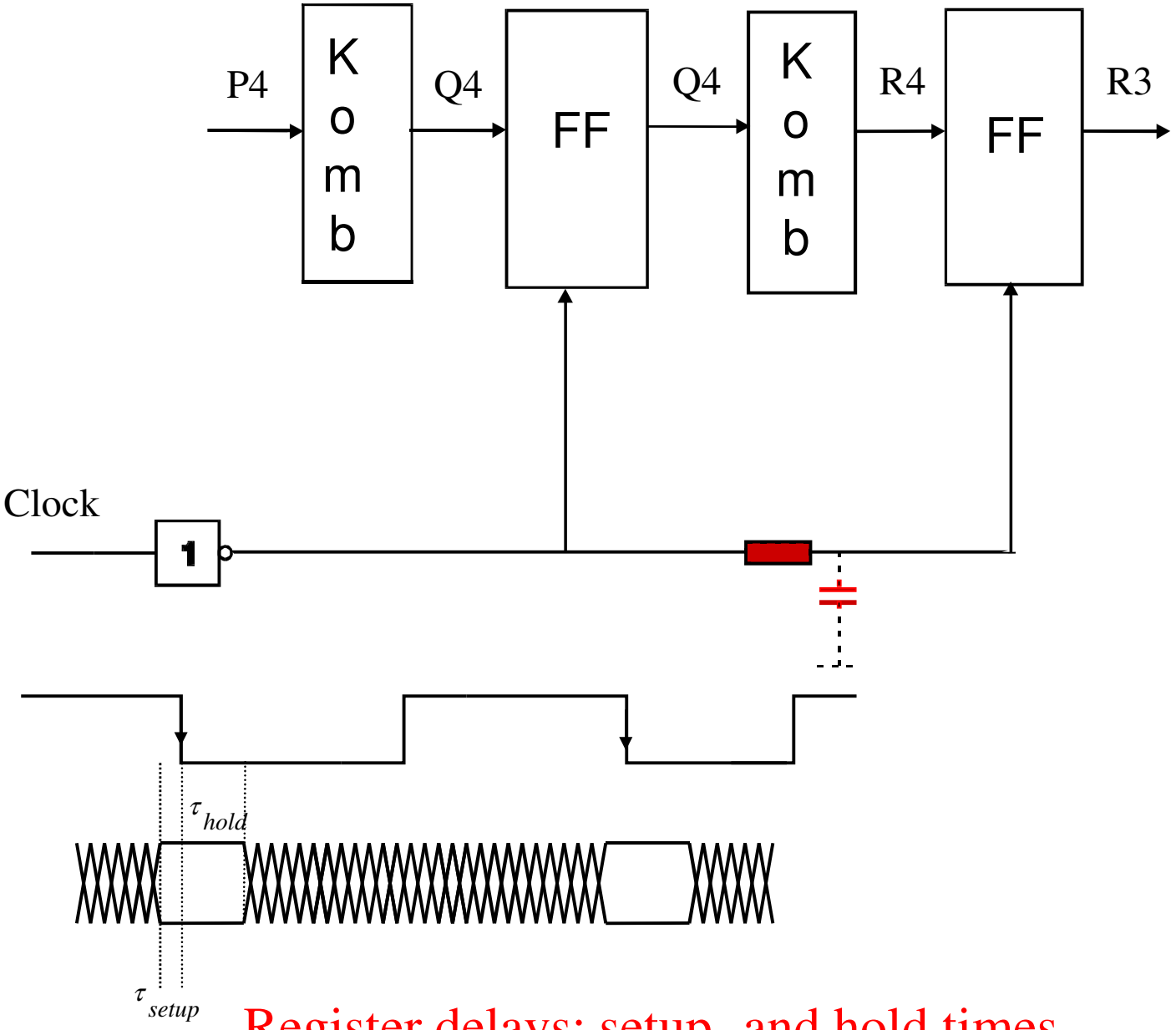

| | | | | | |
|---|---|---|---|---|---|
| Data | P1 | Q1 | | | |
| Clock | P1 | Q1 | Q1 | R1 | |
| Data | P2 | Q2 | Q1 | R1 | |
| Clock | P2 | Q2 | Q2 | R2 | R1 |
| Data | P3 | Q3 | Q2 | R2 | R1 |
| Clock | P3 | Q3 | Q3 | R3 | R2 |
| Data | P4 | Q4 | Q3 | R3 | R2 |

# Clock- / Driver



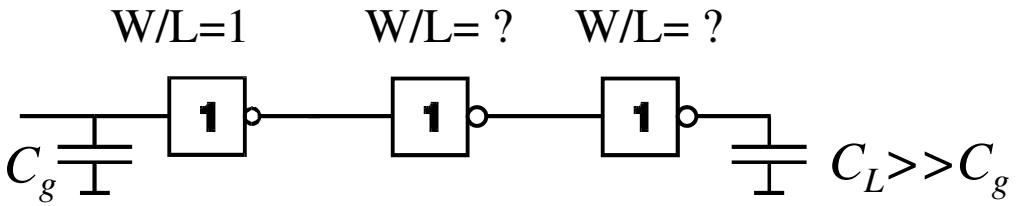

| | | | | | |
|---|---|---|---|---|---|
| | P1 | Q1 | | | |
| Clock | P1 | Q1 | Q1 | R1 | |
| Data | P2 | Q2 | Q1 | R1 | |
| Clock | P2 | Q2 | Q2 | R2 | R1 |
| Data | P3 | Q3 | Q2 | R2 | R1 |
| Clock | P3 | Q3 | Q3 | R3 | R2 |
| Data | P4 | Q4 | Q3 | R3 | R2 |
| Clock | P4 | Q4 | Q4 | R4 | R3 |

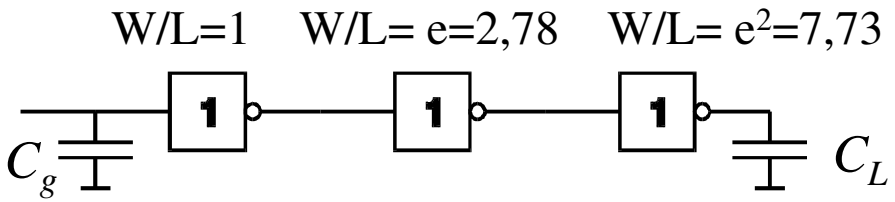
# Clock- / Driver



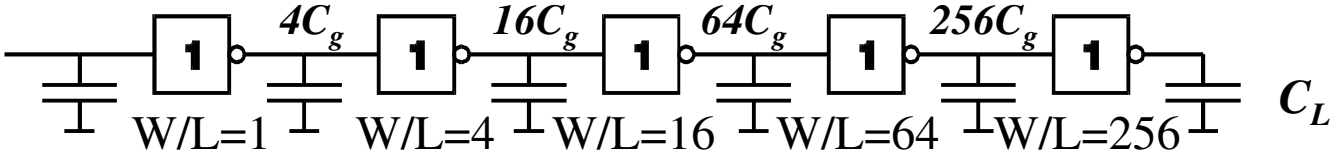

Register delays: setup- and hold times

# Chain of drivers as clock driver



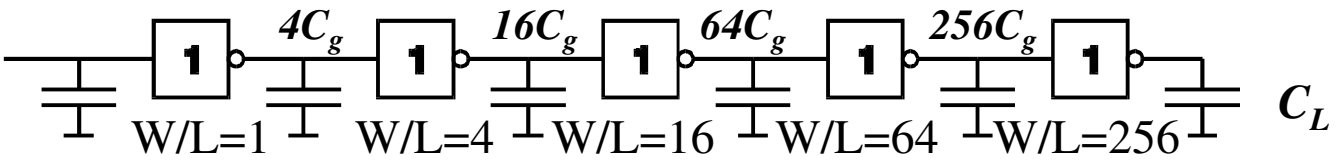




$$number\ of\ stages = Log_n\left(C_L / C_g\right)$$

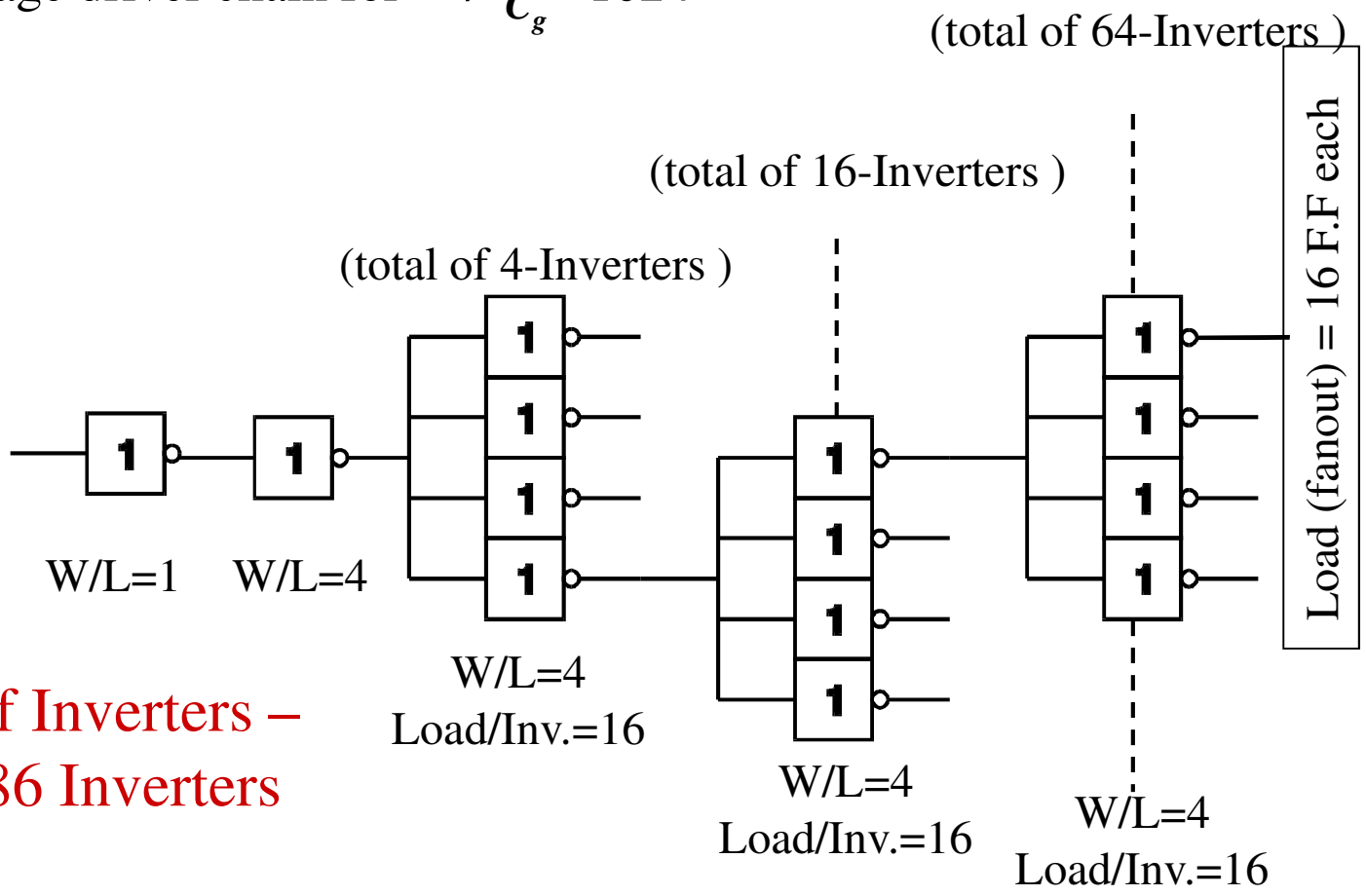



Five stage chain of drivers for $C_L / C_g$ =1024 eg. 1024 Latches or 512 Flip-Flops

# Driver arrangement for clock sub-network

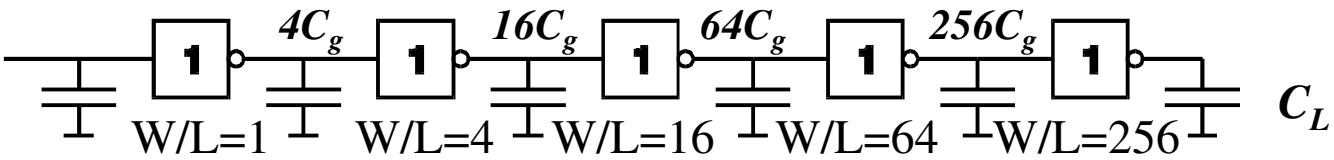



Five stage driver chain for $C_L / C_g = 1024$

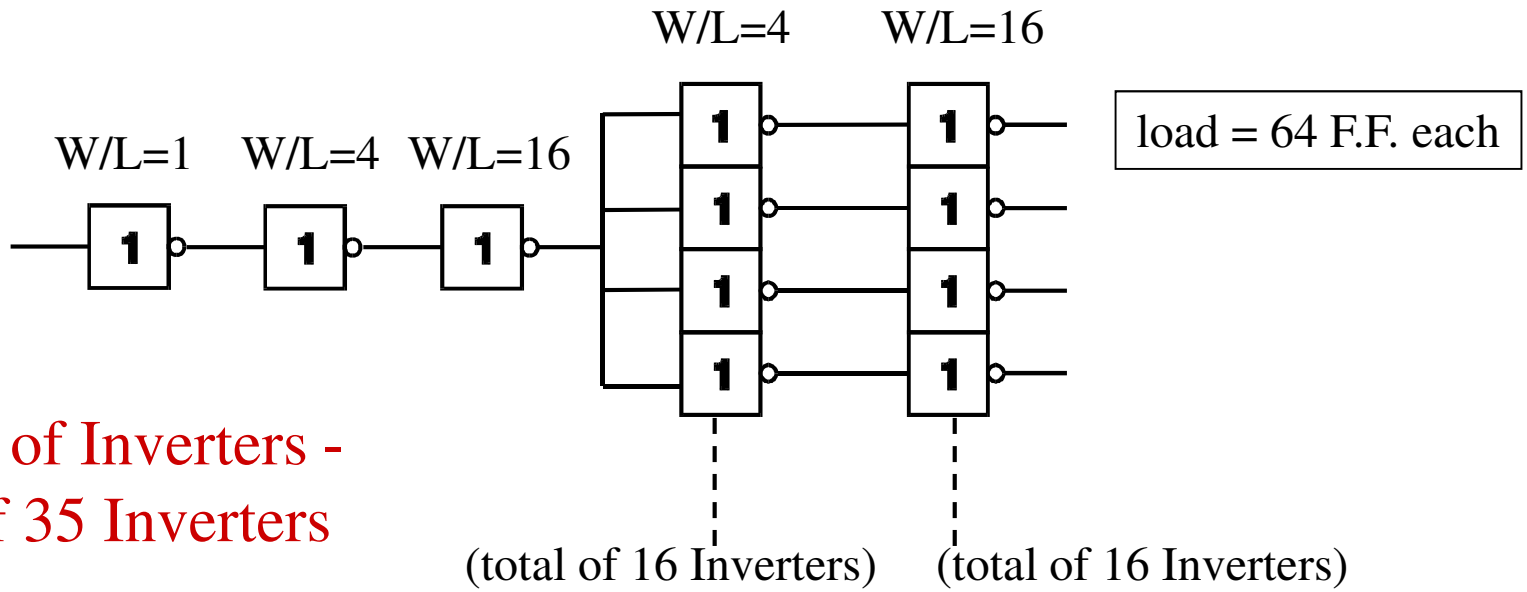



2 Types of Inverters – total of 86 Inverters

# Driver arrangement for clock sub-network (2)




Five stages driver chain for $C_L / C_g$ =1024




3 Types of Inverters -
total of 35 Inverters

# Clock Design

Compromise between

- Robustness and complexity
- Constraints of Logics versus Constraints of Clock

Clock Method:

- Pulse control
- Edge control
- Single-phase Clock
- Two-phase Clock

# Comparison Clock-Method

## Pulse mode

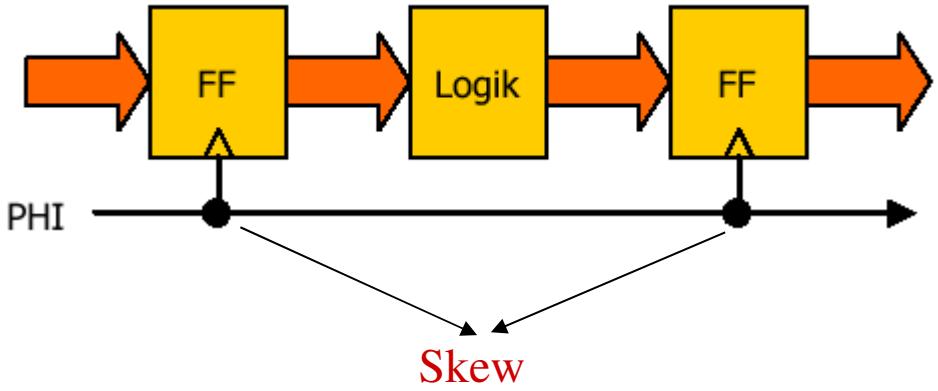
**+ simple**

**- Signal delay time should not be too big or too small**
**- Pulse width critical (50%)**

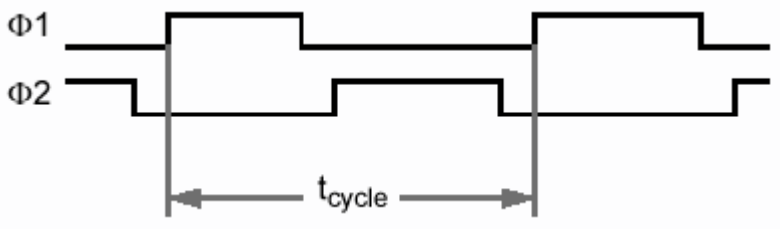
## Edge control

**+ more robust than pulse mode**

**- Skew of Clock signals on each FF/Registers can be a problem**




Solution: two-phase Clock



# 11. Sequential Circuits

1. Realization of Registers
   (Latches, Flip-Flops)
   1. Dynamic Registers
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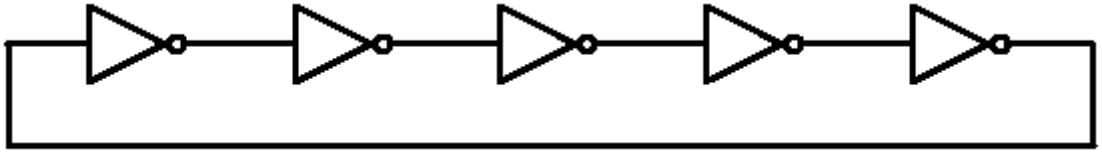
2. Pipeline
3. Clock Distribution – Clock Networks
4. **Clock Generation**

# Principle of Ring Oscillator



Inverter chain with feedback

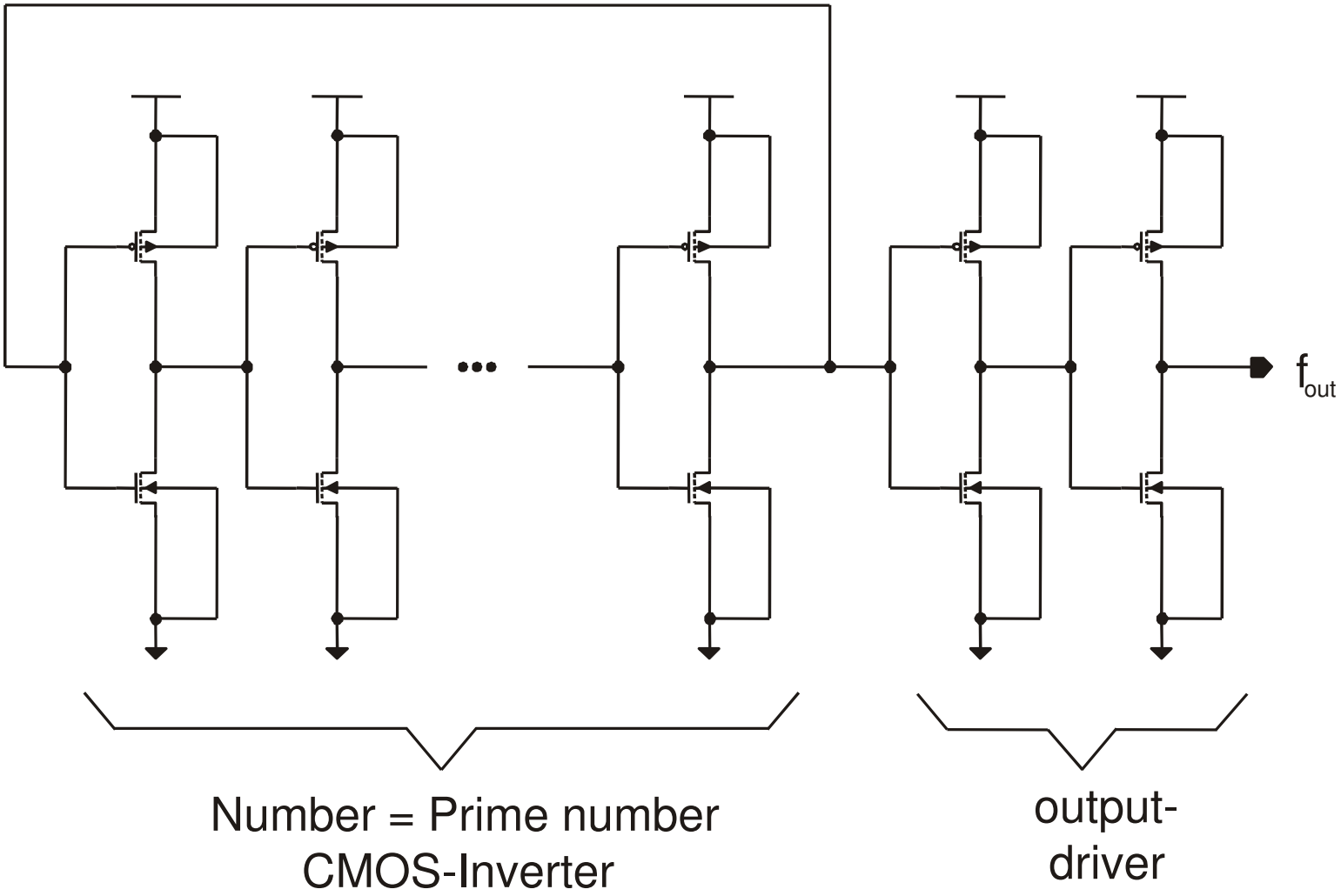
Odd number of inverters in the loop

How would it be with an even number? Latch

Periode of the oscillator ? n*delay time of inverter

The number of inverters has to be a prime number.

# Ring oscillator circuit



# Realization for clock generation

## 1) Ring oscillator

+ pure integrated solution
- Subject to frequency, temperature and process variations

Ring oscillator is used in PCM

## 2) RC-Oscillator

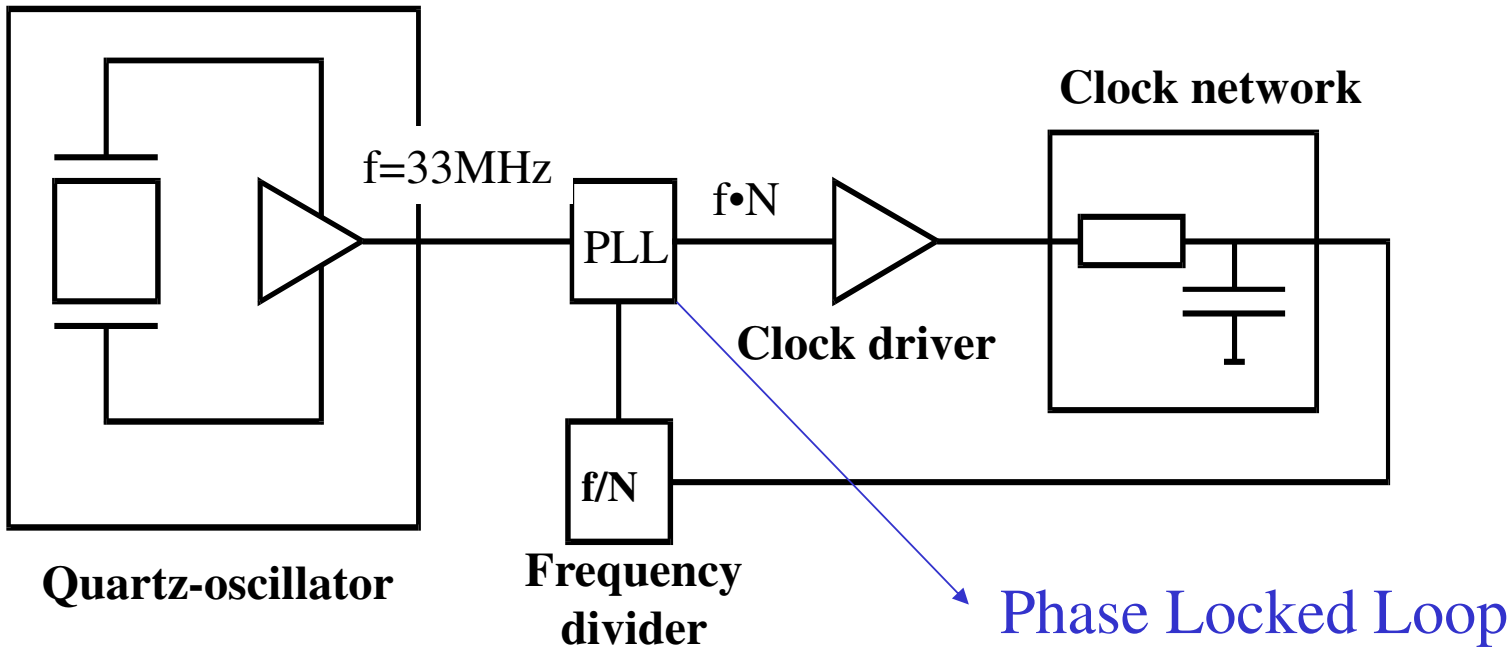
External components are necessary (R, C resp. Resonator),
Frequency accuracy in percentage range

## 3) Crystal/Quartz

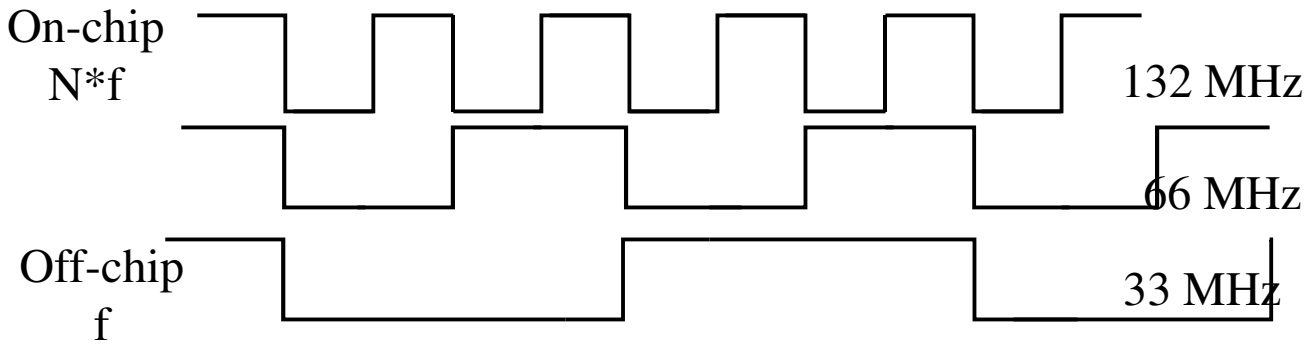
+ extremely accurate frequency
- expensive

Frequency of resonator and quartz is in MHz-range

# Clock reproduction




Generation of clock signal



# Composition of a Chip

**12. Periphery of a chip**

1. **Input-Pads**
2. **Output-Pads**
3. **Tri-State-Driver**

**13. Arrangement of components on a chip**

# Requirements on in- and outputs

ESD-protection

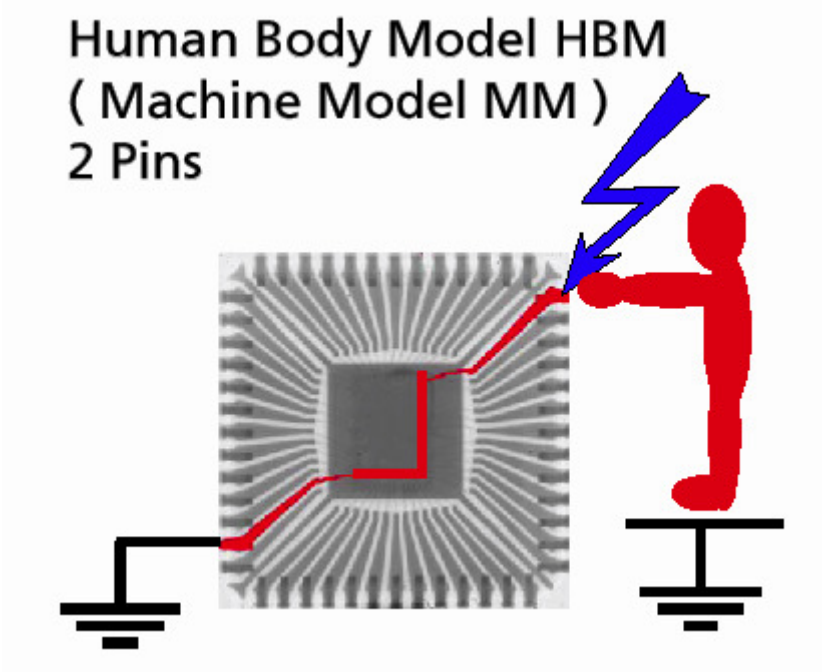
Mixed in- and output

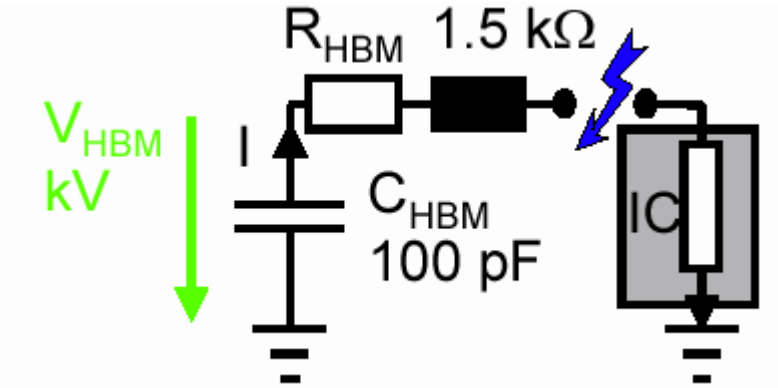
Level shifter

Analog-Digital converter (input)
and Digital-Analog-converter (output)

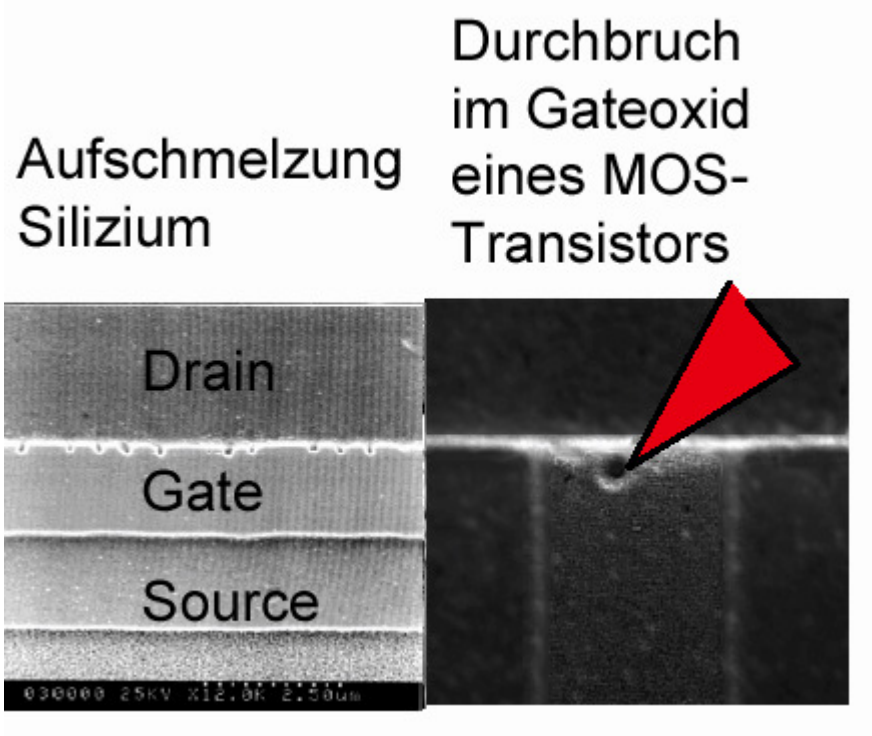
Tristate, Common drain output

# ESD Stress Model

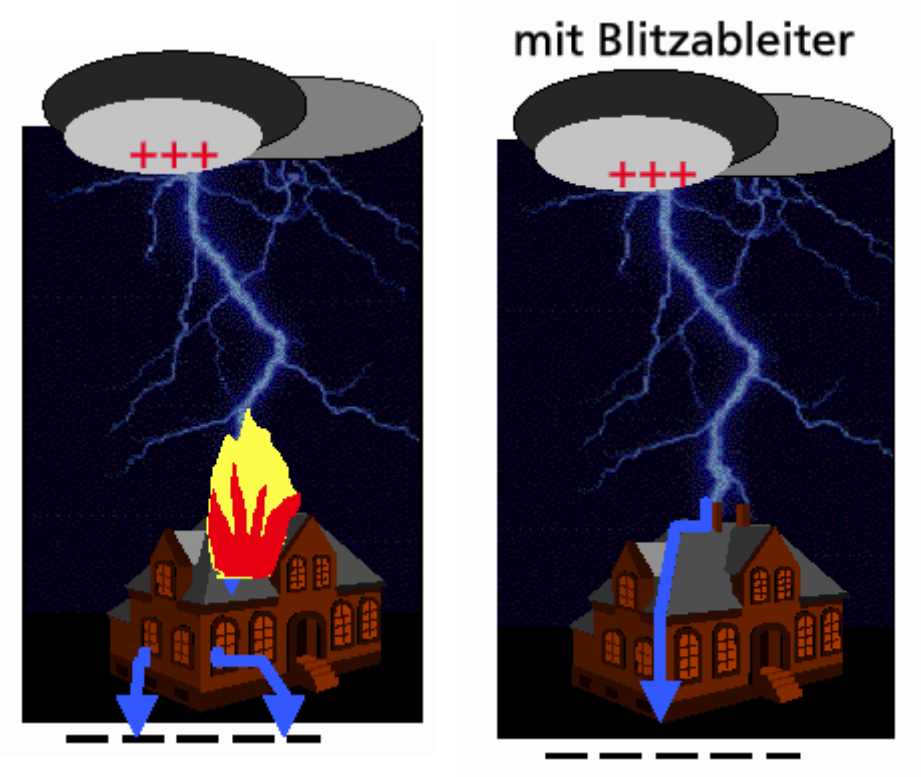


# Effects: Damages in integrated circuits



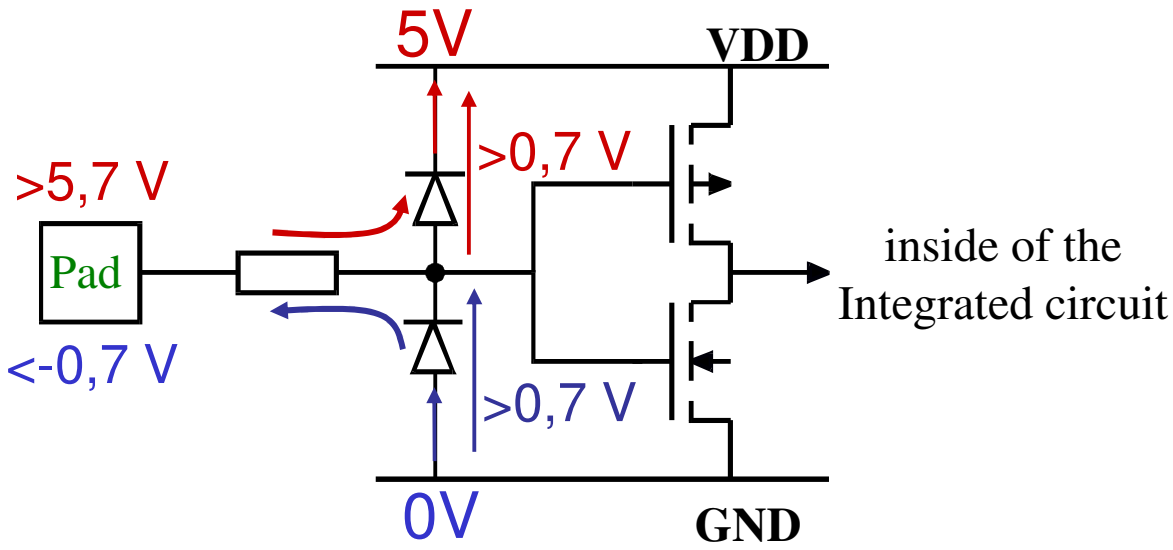

Destruction of the thin Gate




Equal to Phenomenon lightning

Solution

# ESD-Protective Circuit




Input-Pad with protective circuit

ESD-voltage (e.g. 2 kV) and energy is dissipated in ESD-resistor (1,5 kΩ) and the Pad-resistor.

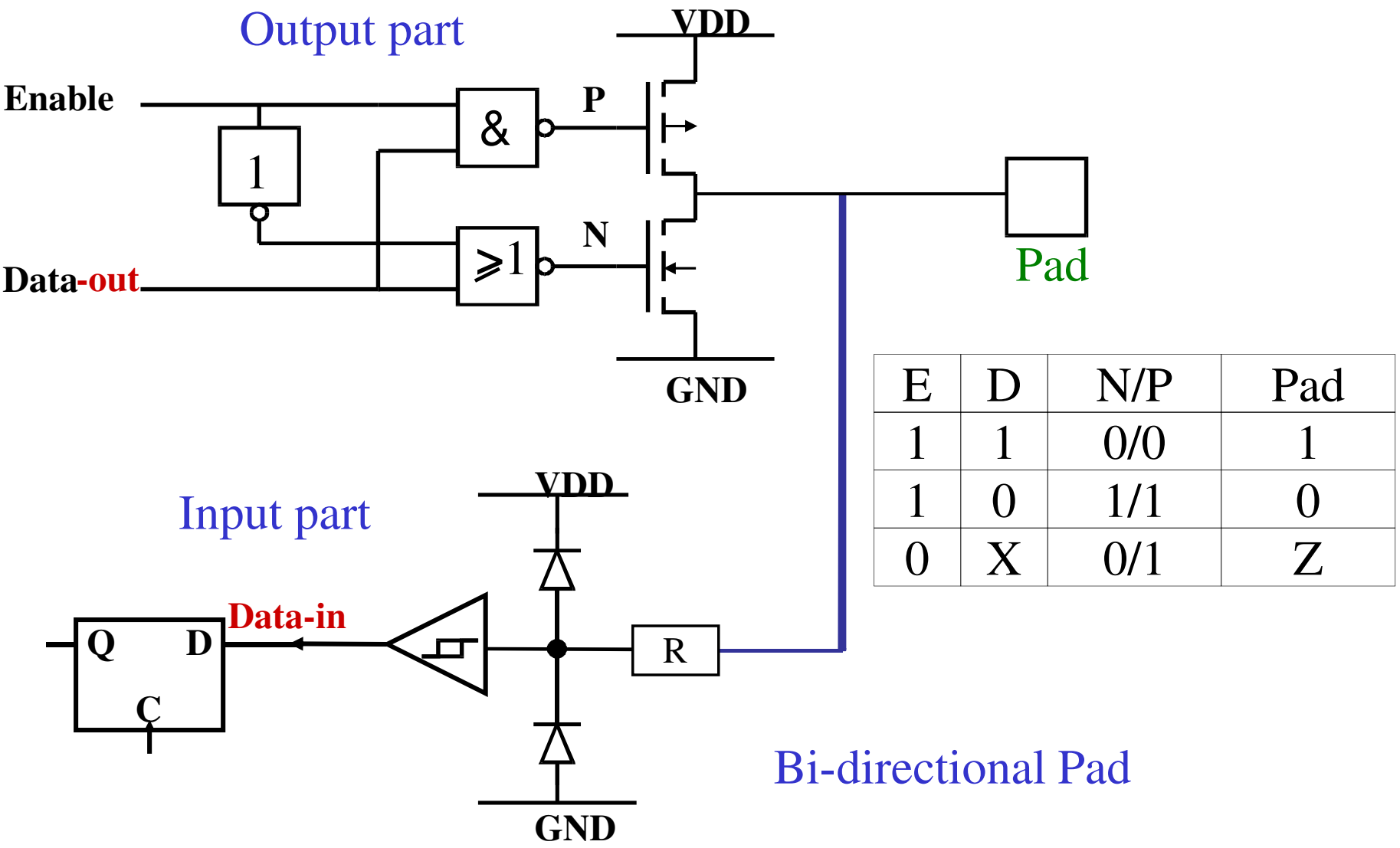
The gates at the input must not receive high voltage.

Modern ESD-protection circuits use transistors instead of diode.

For digital circuits ESD-protection including layout is included in Pad-Library.

For special analog pads (HF, HV etc.) a proprietary design is needed.

# Mixed In- and Output + Tri-State-Pad



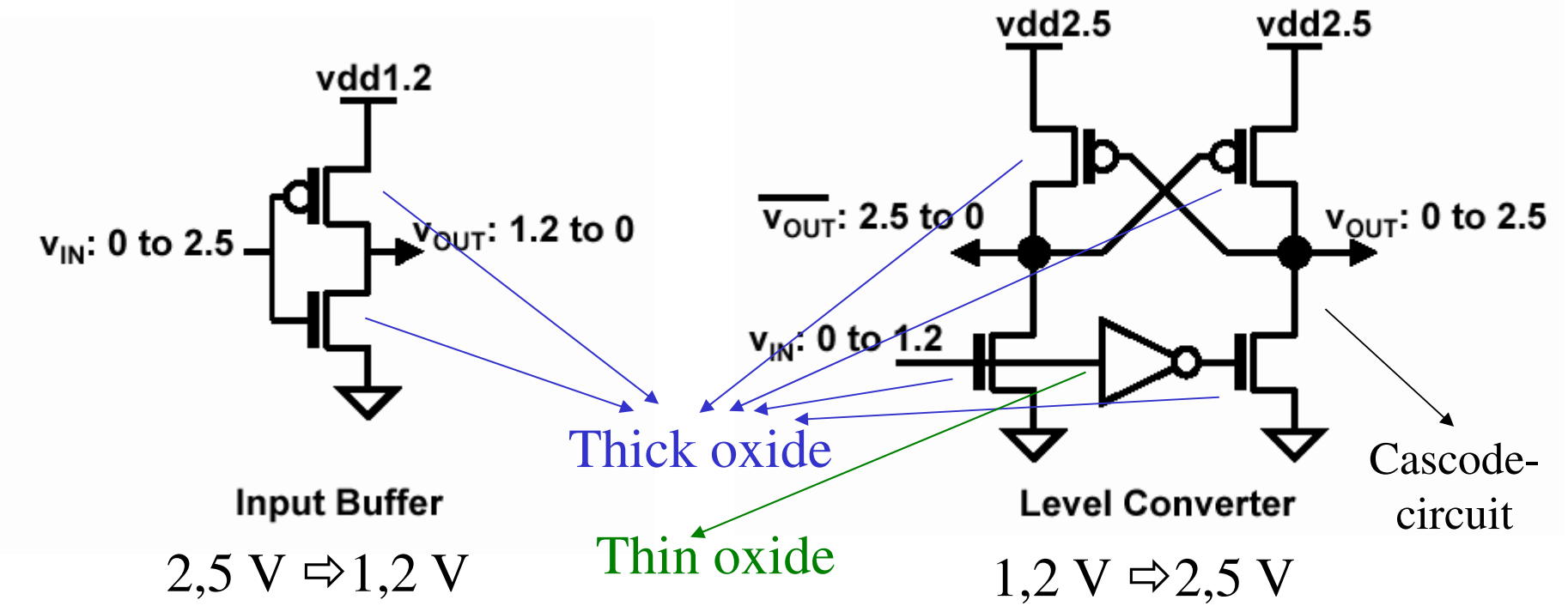

| E | D | N/P | Pad |
|---|---|---|---|
| 1 | 1 | 0/0 | 1 |
| 1 | 0 | 1/1 | 0 |
| 0 | X | 0/1 | Z |

# Level Shifter

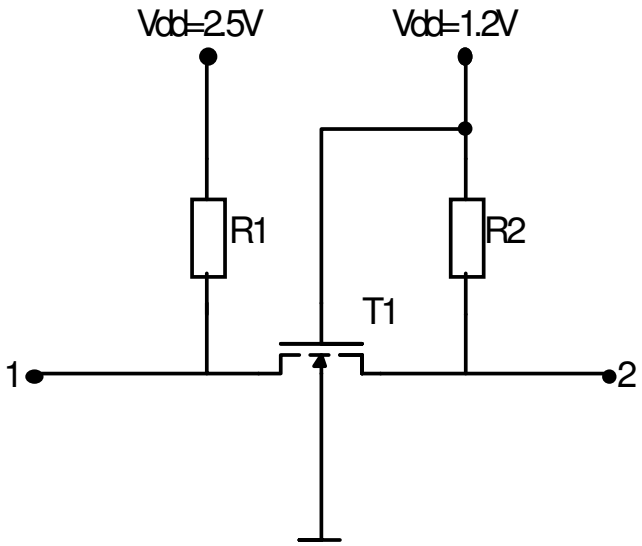
A modern IC process has always two gateoxides
with two voltage classes (e.g. 1,2 V / 2,5 V)

In- and outputs are operated with higher voltage,
whereas the inner logic-core receives only low voltage.

A conversion between these voltages is therefore necessary.



# Level converter for mixed in-and outputs

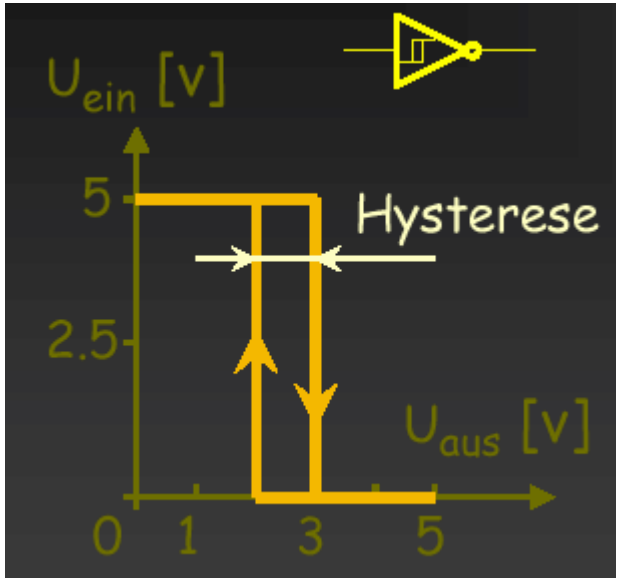



Common Gate Circuit

| | | | |
|---|---|---|---|
| Input | node 1 | 0 | 2.5 |
| Output | node 2 | 0 | 1.2 |
| T1 | | on | off |
| I(T1) | | 1.2/R2 | 0 |
| i(input) | | 2.5/R1+1.2/R2 | 0 |

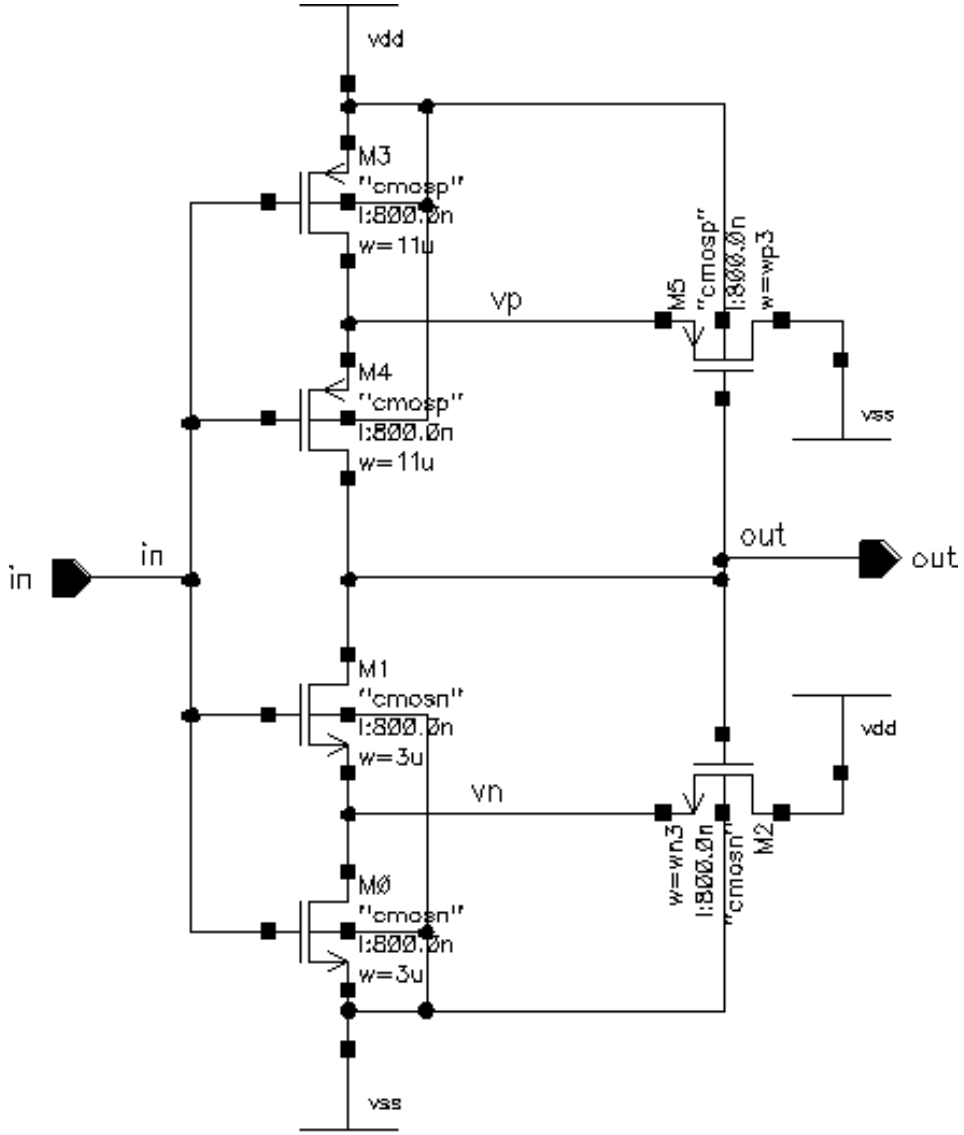
| | | | |
|---|---|---|---|
| Input | node 2 | 0 | 1.2 |
| Output | node 1 | 0 | 2.5 |
| T1 | | on | off |
| I(T1) | | 2.5/R1 | 0 |
| i(input) | | 2.5/R1+1.2/R2 | 0 |

# Schmitt-Trigger



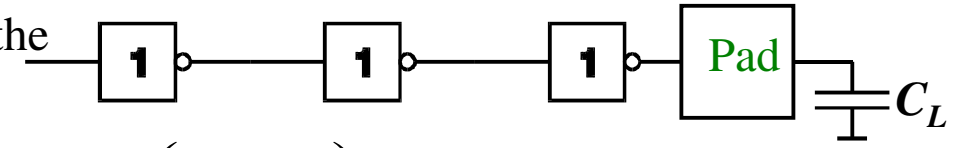

Hysteresis suppresses noise/ disturbances at input and prevents Oscillation at output

„1 Bit Analog-Digital-converter“



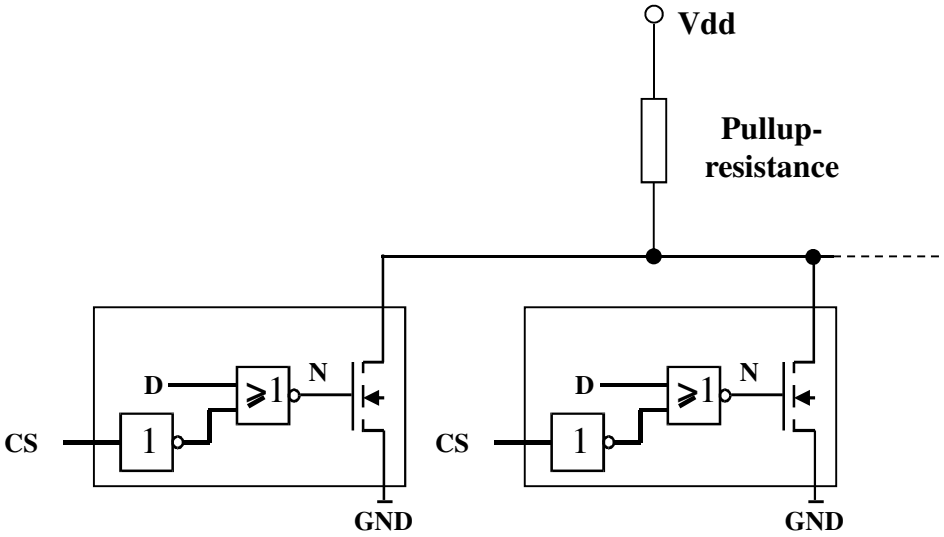
# Output driver-I/O-Driver

From the inside of the Circuit

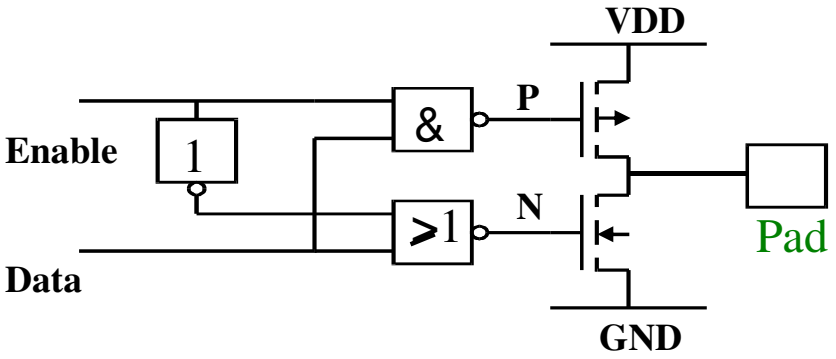



$$\ln\left(C_L / C_g\right)$$

Output-Pad




Open Drain Output




Tristate Pad

# Arrangement of Pads, Logics, Clock- and Supply lines on a Chip