Chapter15 Flipflop-Circuit

1. Counter
2. Register

Chapter 16 Memory

1. RAM - Random Access Memory
   static RAM (SRAM)
   dynamic RAM (DRAM)
2. NVM (non-volatile memory)
3. ROM - Read Only Memory

Standard Logic Devices

1. PLA – Programmable Logic-Arrays
2. FPGA

Digital Counters

Applications?

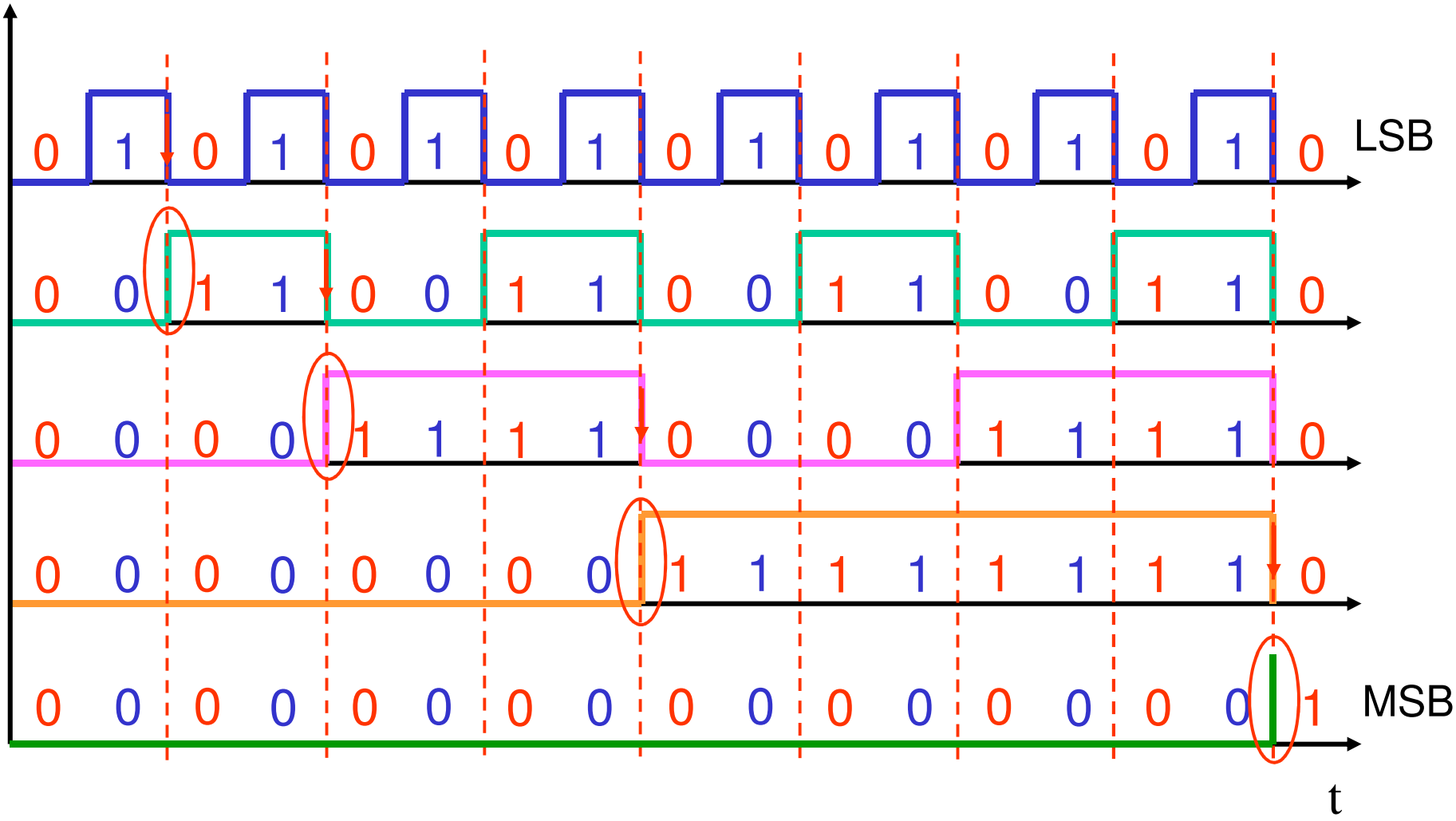
Counters are needed for:

Program counter	Microcontroller-embedded Systems
Event counter	Sensors and Aktors, Programs (if i=x then ...)
Frequency divider	Core Clock <> System Clock

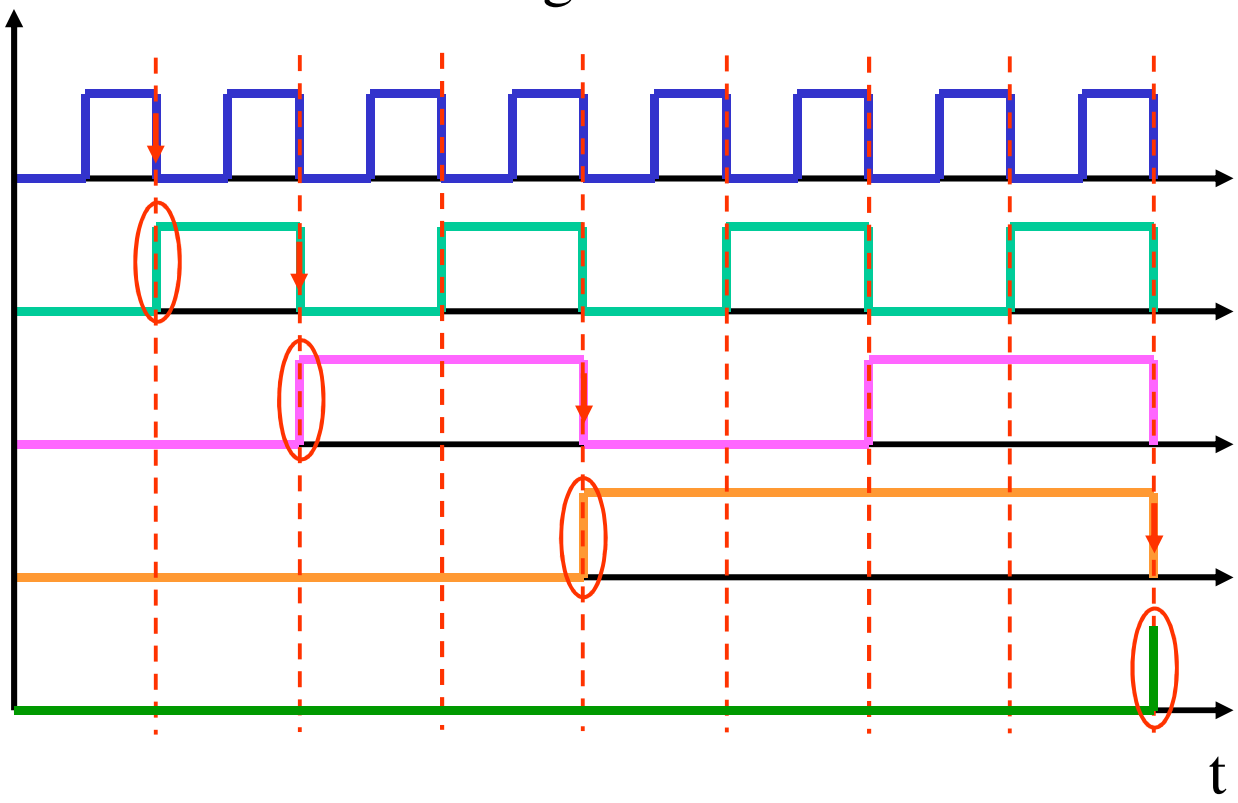
System clock may be a reference event (insusceptible to disturbances).

Thermally stabilized (TCXO)

Digital Counters

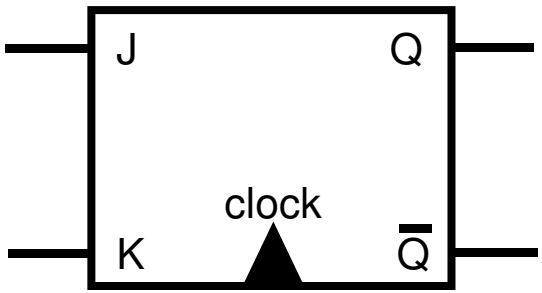


Digital Counter-Realization

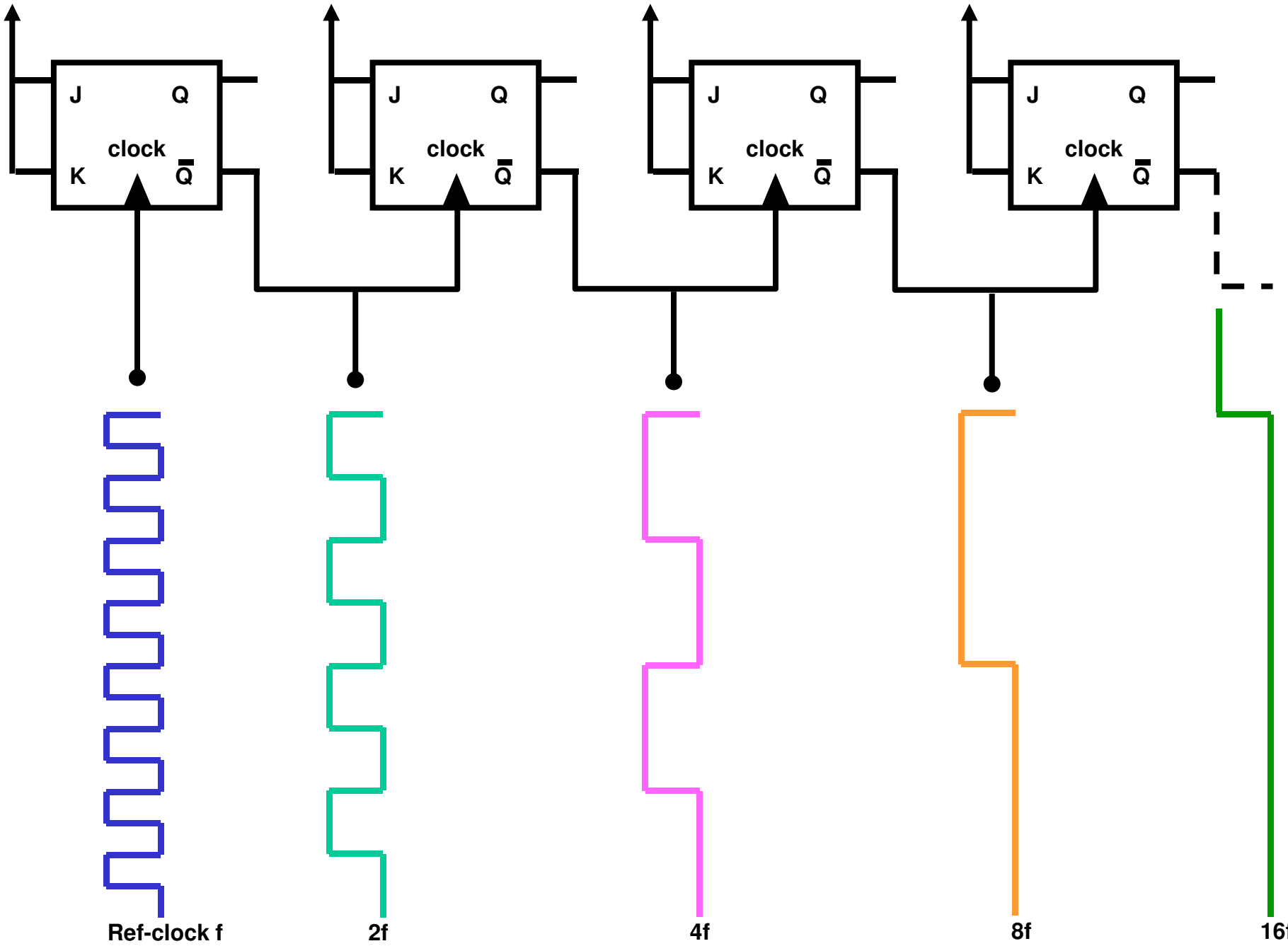


Stage changes with fallen edge of the next lower bits, otherwise storage of the current value.

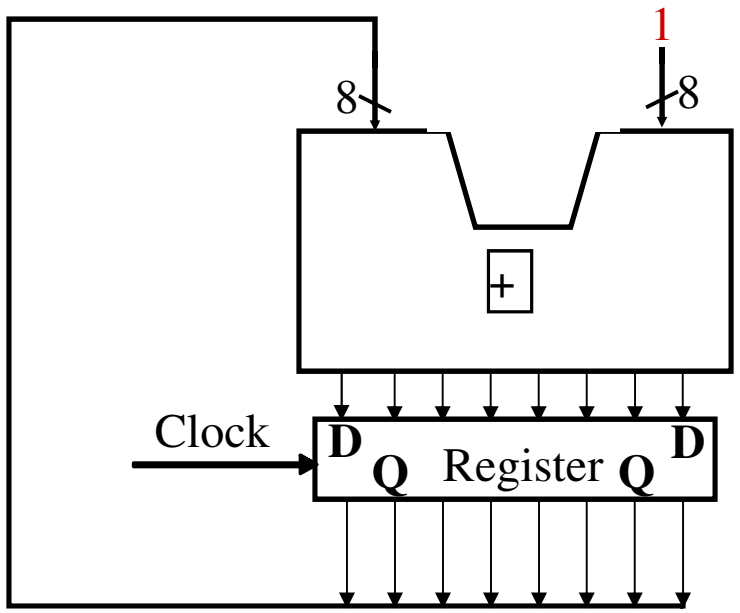
Device: egde-controlled JK-Flip-Flop



J	K	Q_n ⎍	Q_n ⎎
0	0	$\mathbf{Q_{n-1}}$	$\mathbf{Q_{n-1}}$
0	1	$\mathbf{Q_{n-1}}$	0
1	0	$\mathbf{Q_{n-1}}$	1
1	1	$\mathbf{Q_{n-1}}$	$\mathbf{\overline{Q}_{n-1}}$


J
Q
clock
K
Q
J
Q
clock
K
Q
J
Q
clock
K
Q
J
Q
clock
K
Q
Ref-clock f
2f
4f
8f
16f

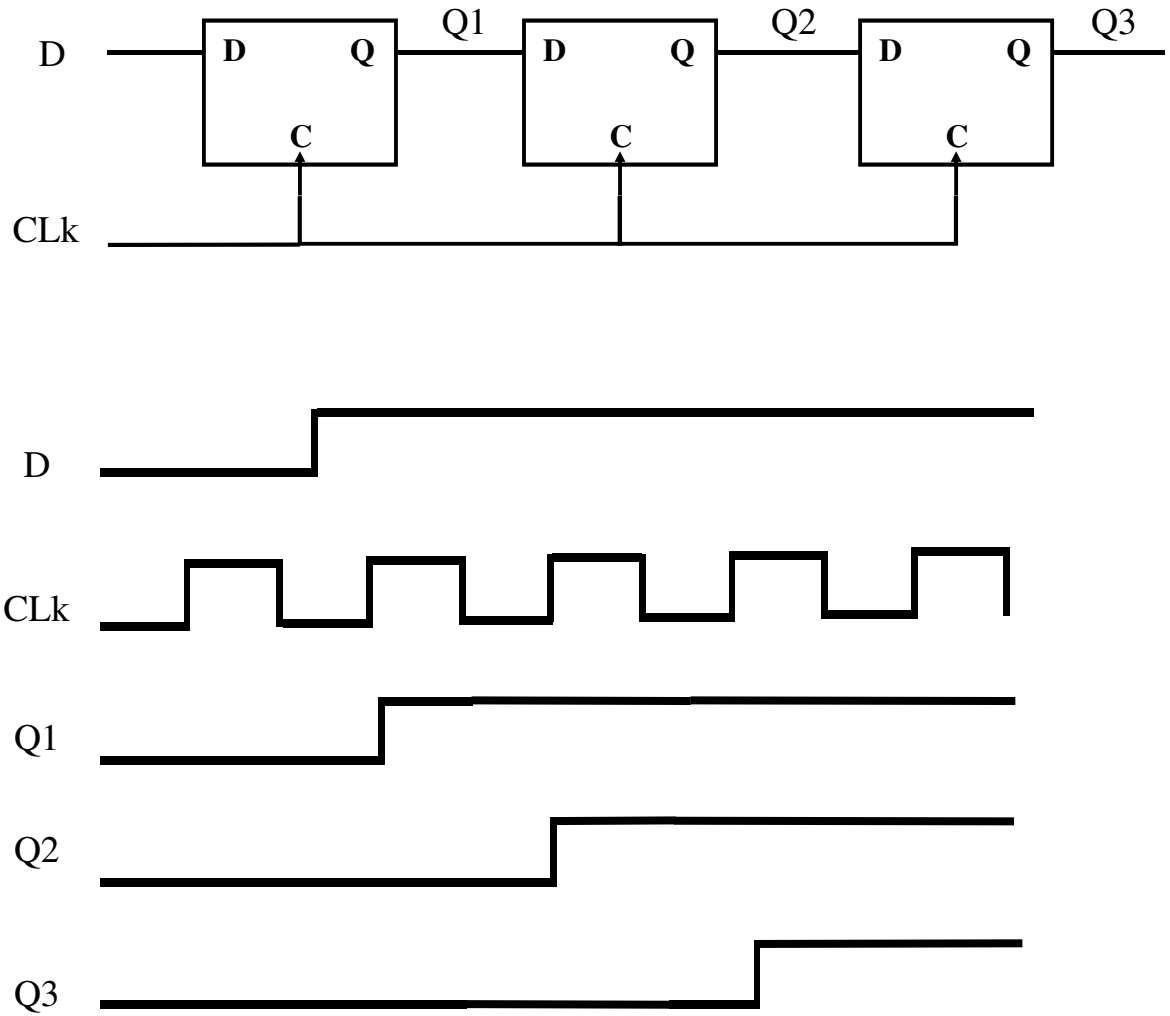
State storage



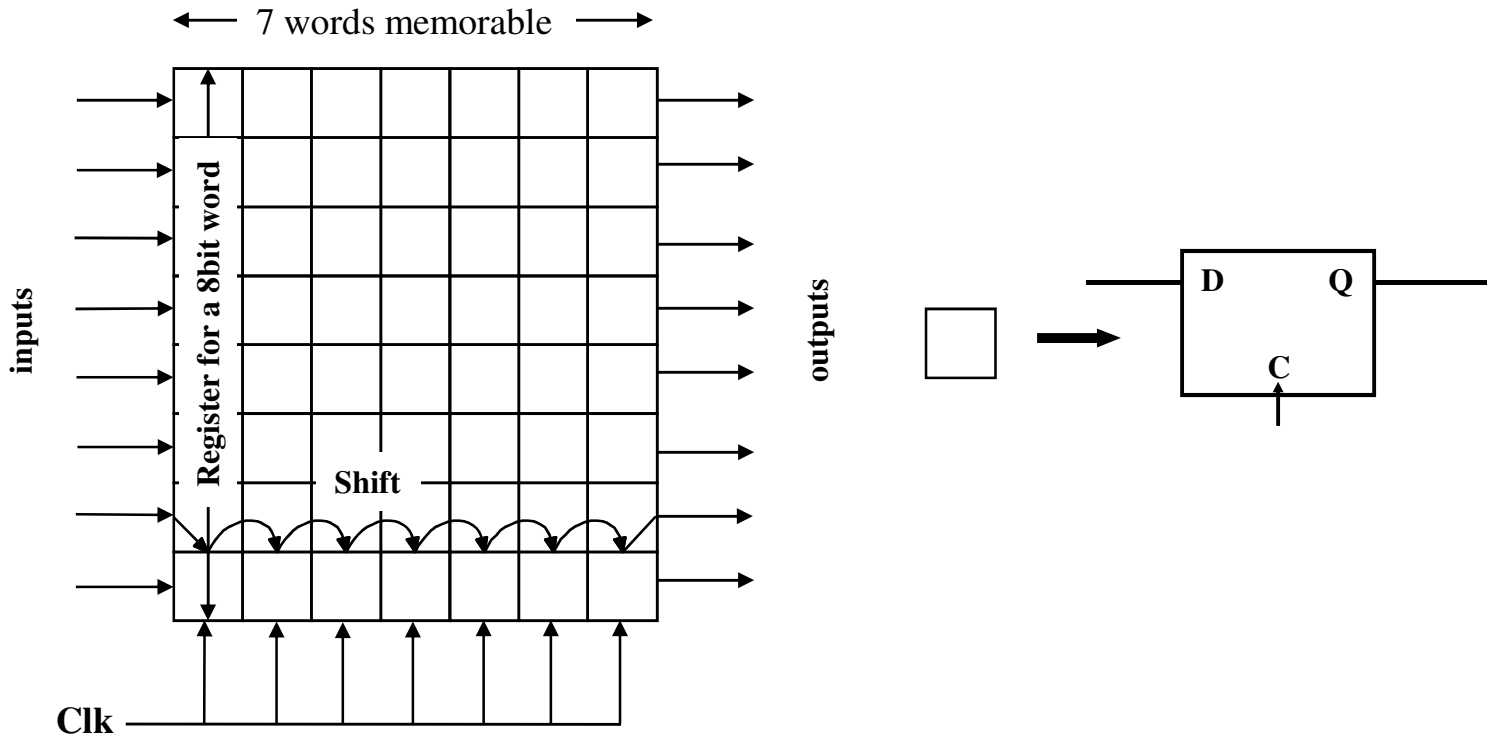
Accumulator / Incrementer

Parallel Register

Shift register (FIFO)



FIFO memory with word width of 8 bit and depth of 7



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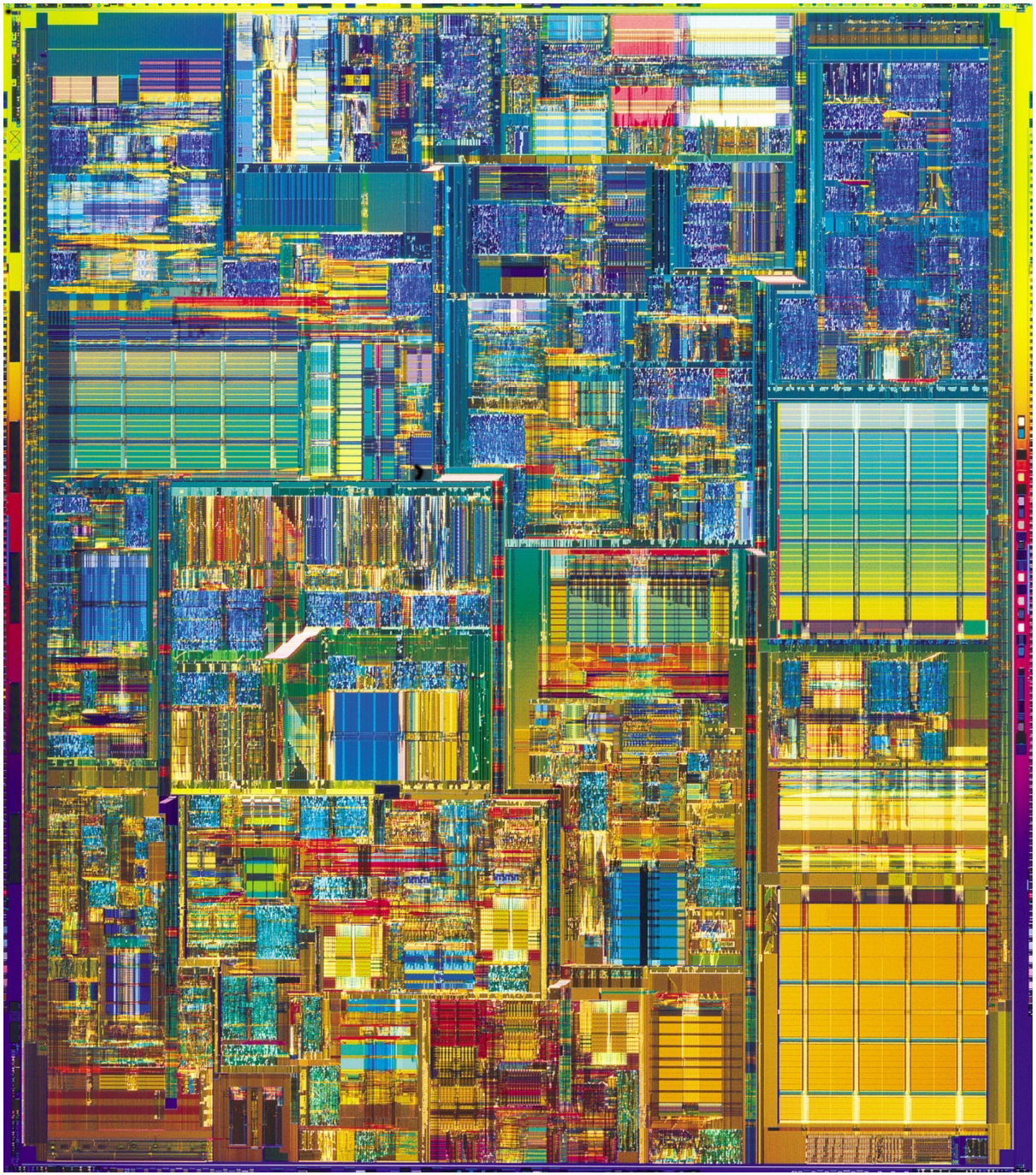
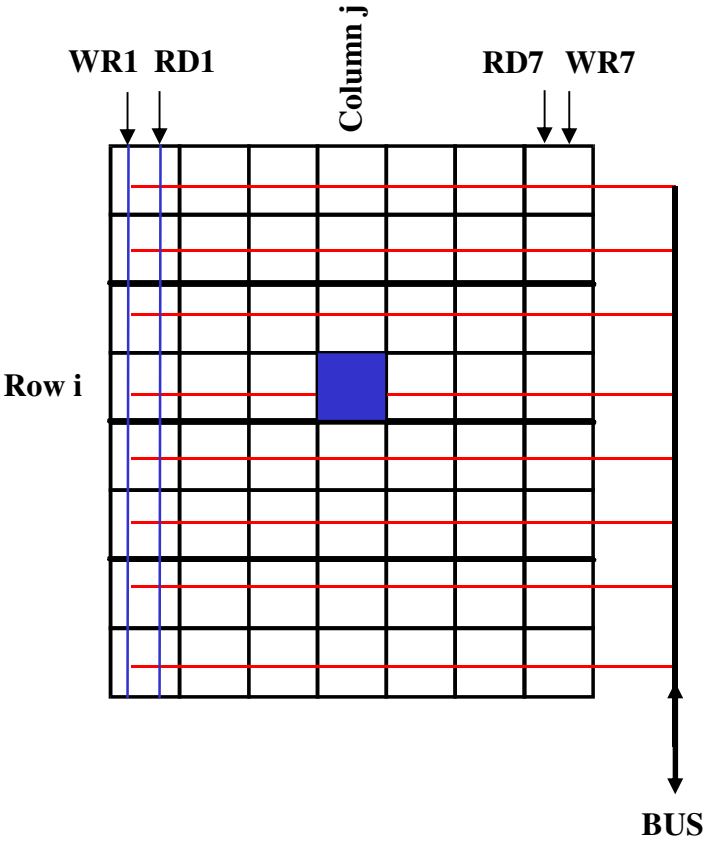
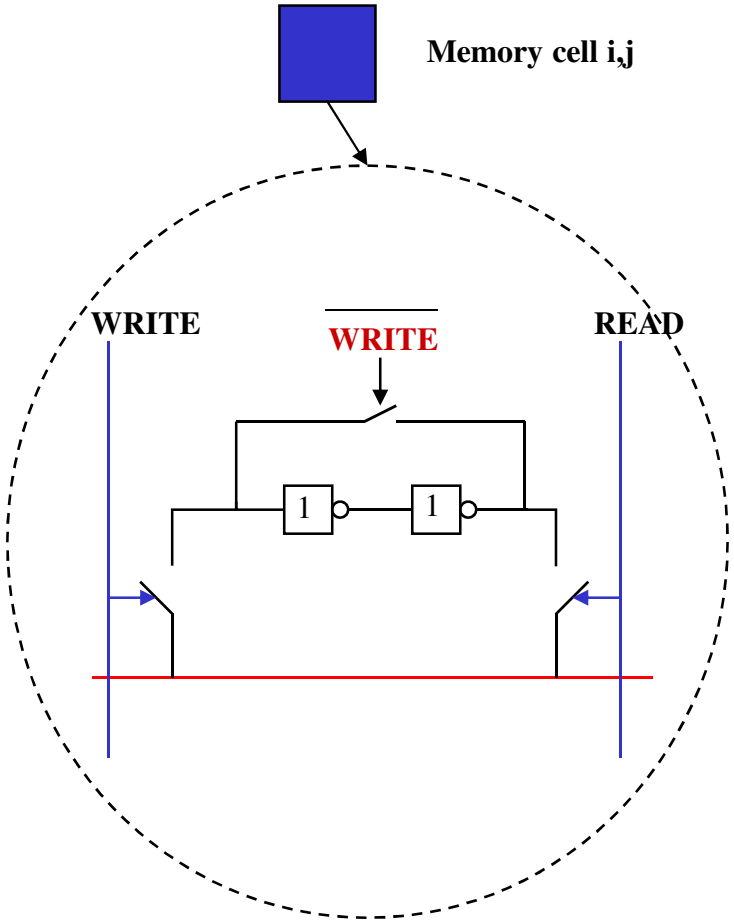
Pentium 4

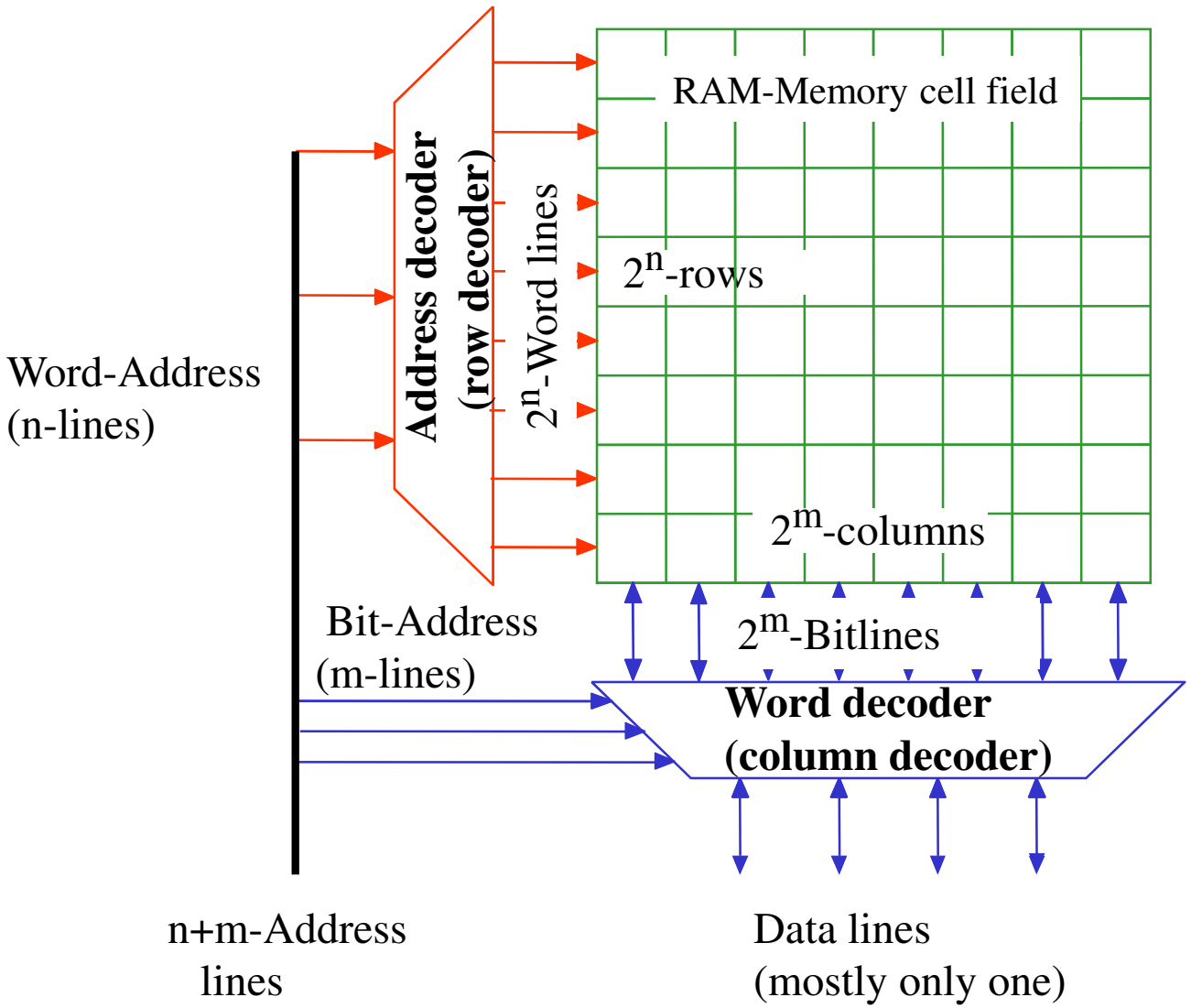


Schematic Structure of a Memory-Array

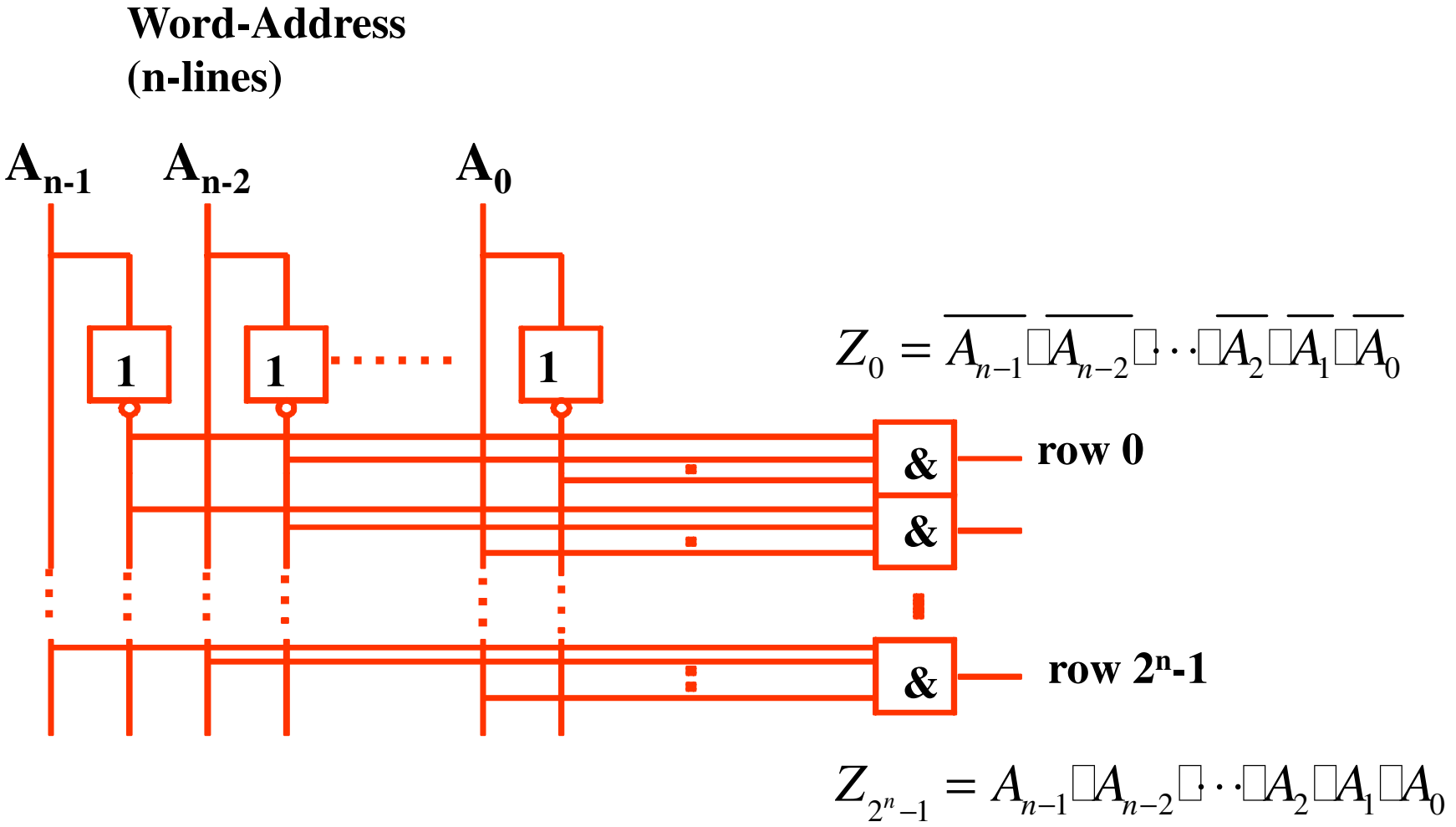




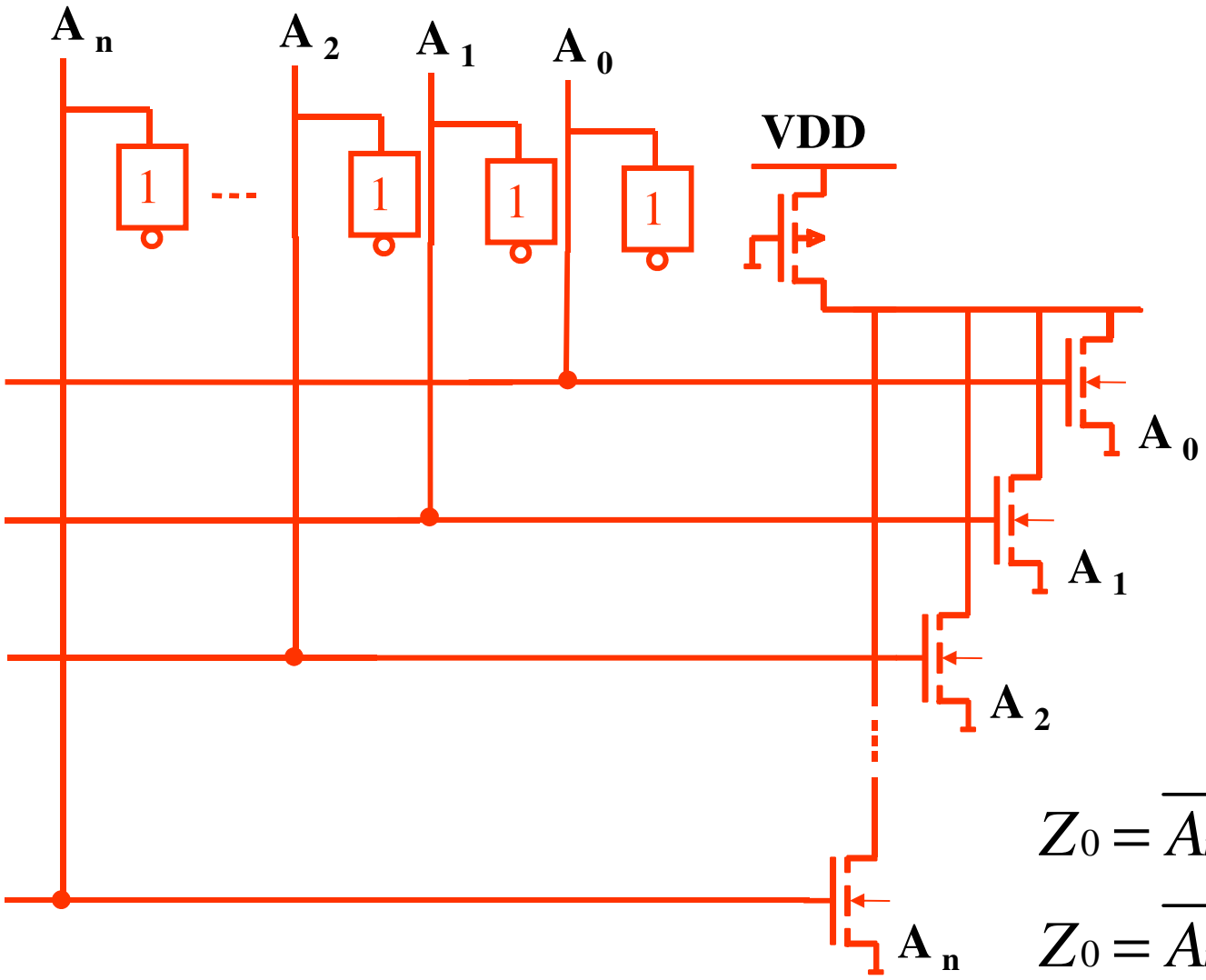
Schematic Structure of a RAM



Functional Structure of a Row Decoder



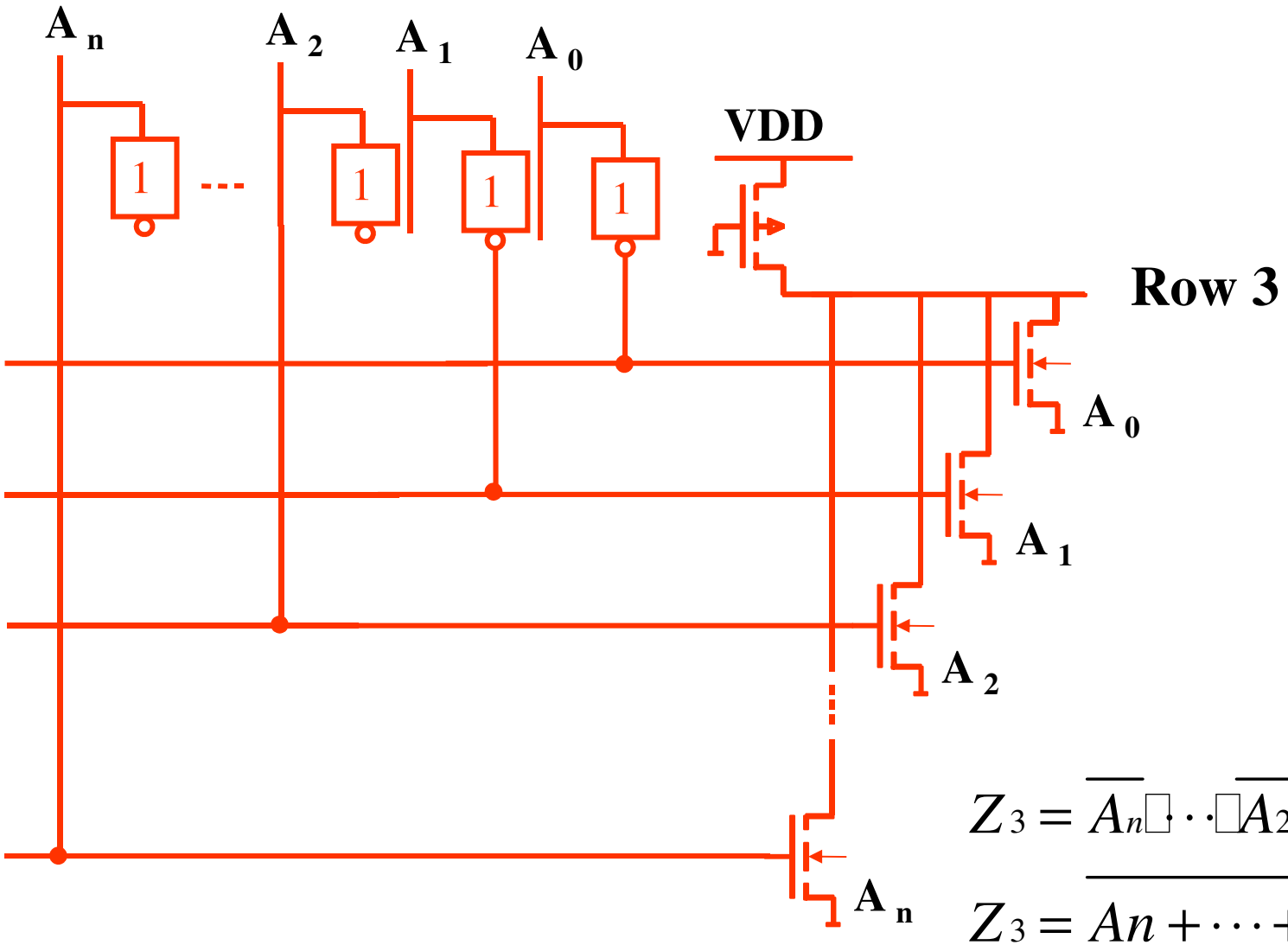
Structure of a NOR in Row Decoder for row 0



$$Z_0 = \overline{A_n + \cdots + A_2 + A_1 + A_0}$$

$$Z_0 = \overline{A_n} \cdot \cdots \cdot \overline{A_2}\,\overline{A_1}\,\overline{A_0}$$

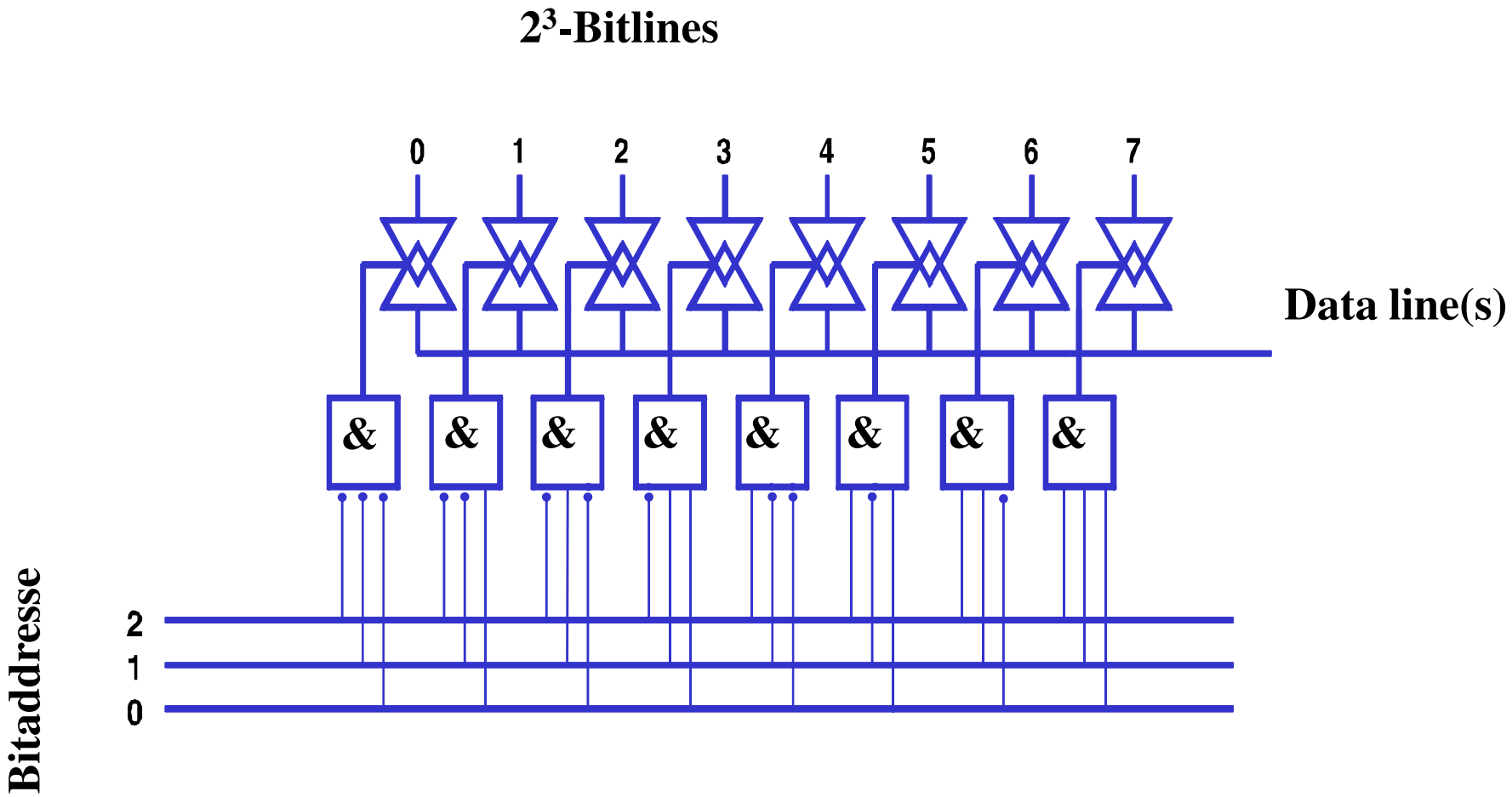
Structure of a NOR in Row Decoder for row 3



$$Z_3 = \overline{A_n} \cdot \cdots \cdot \overline{A_2} \cdot A_1 \cdot A_0$$

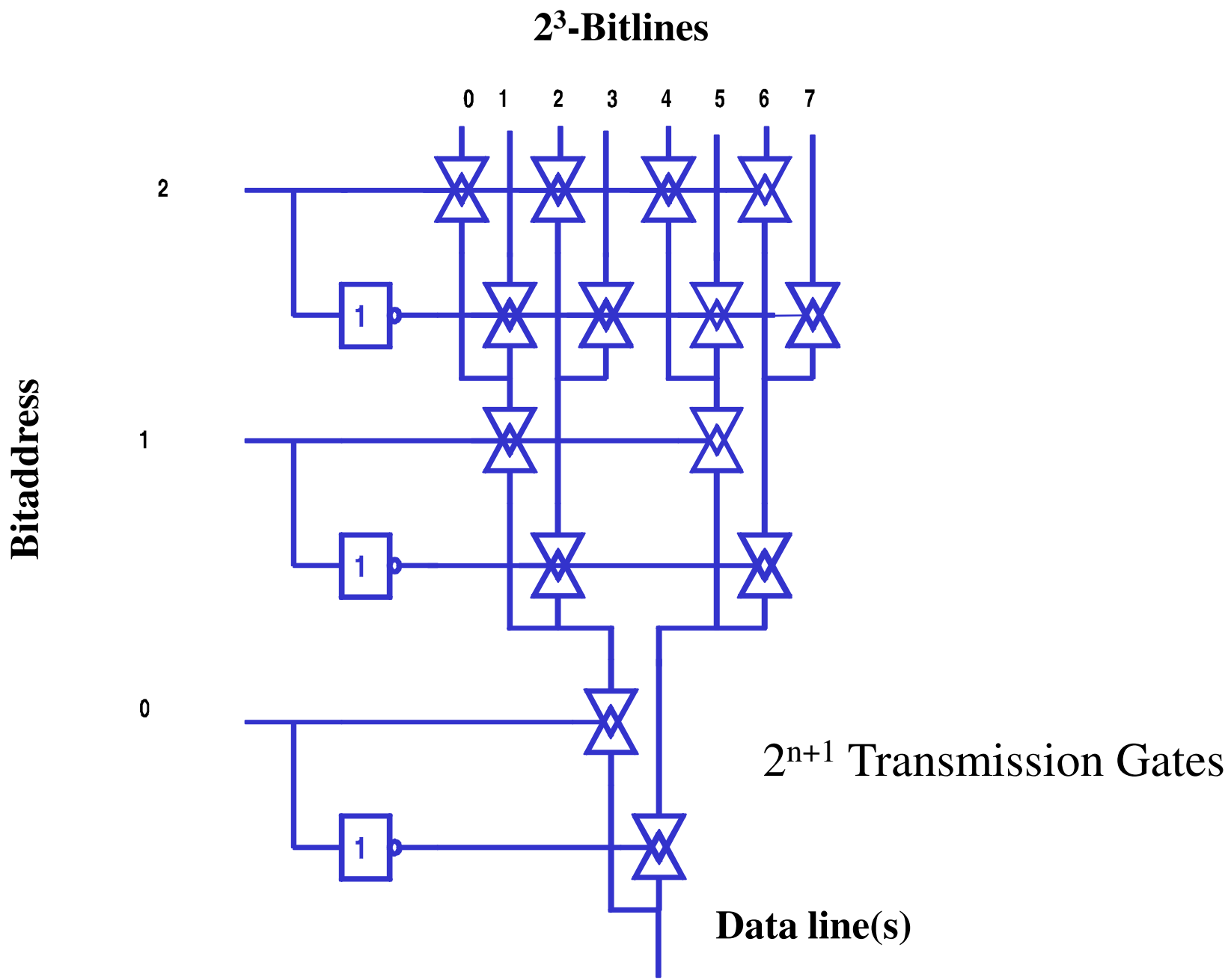
$$Z_3 = \overline{An + \cdots + A2 + \overline{A1} + \overline{A0}}$$

Structure of a Column Decoder

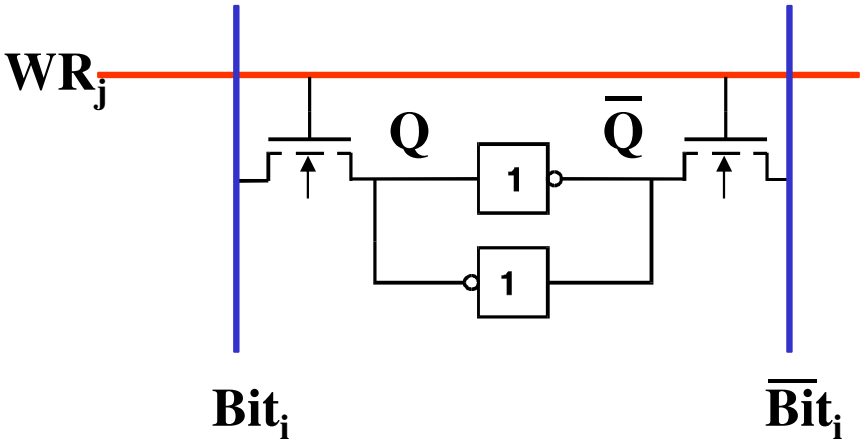


2^n Transmission Gate and 2^n AND with n-inputs

Column Decoder as Multiplexer



RAM-Cells - Static



Static 6-Transistor-RAM-Cell

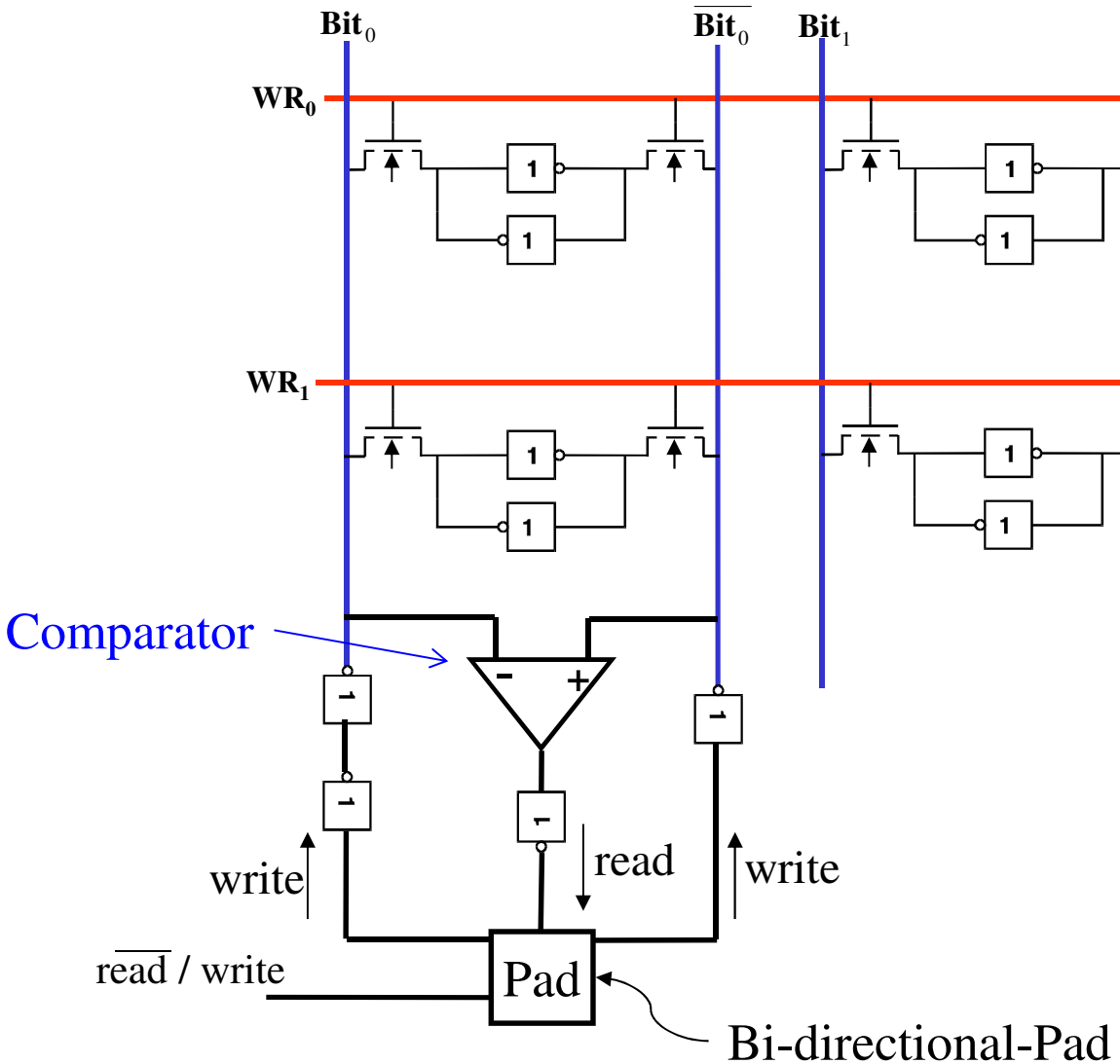
WRj =1	Select read and write
WRj = 0	no activity, only storage

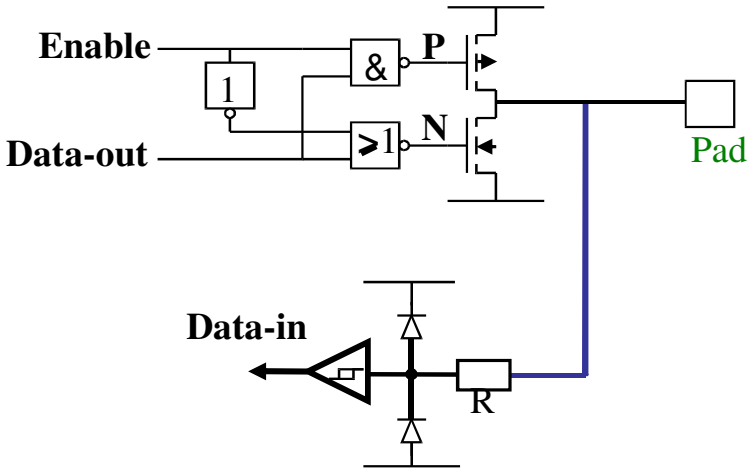
For writing: Q = Bit, Latch is overturned

For reading: $Q = 0 \Rightarrow Bit = 0;\ 1 > \overline{Bit} > 0$

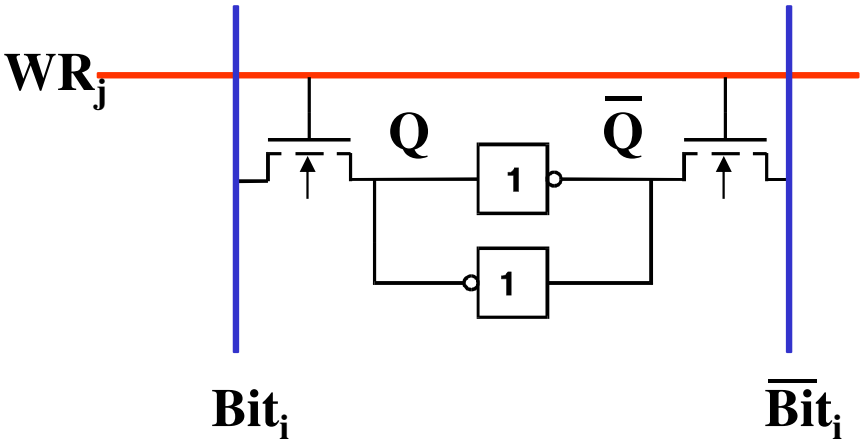
$Q = 1 \Rightarrow 1 > Bit > 0\ ;\ \overline{Bit} = 0$

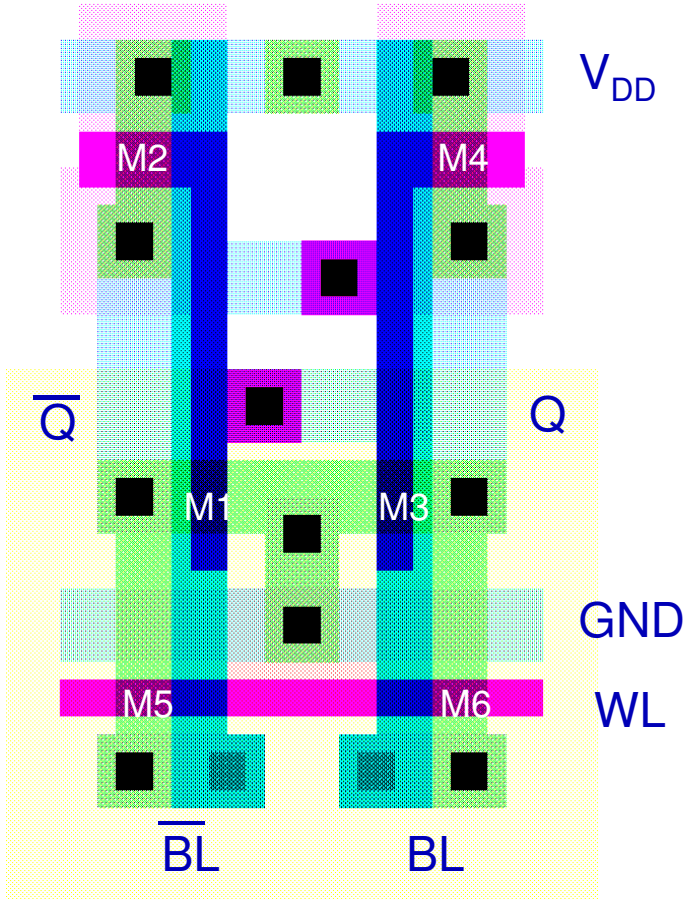
Read-Write-Circuit





SRAM-Cell-Layout

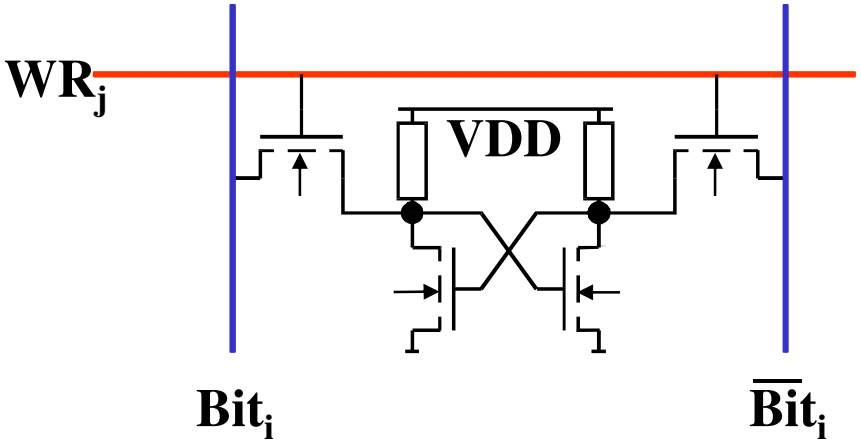




Specifics:

- extremely dense
- general Design Rules are violated
- SRAM designs are produced by Generator SW. Inputs: size, form, connections etc. Supplier: IP Vendor
- SRAM cell is the mostly used unit in a digital chip!

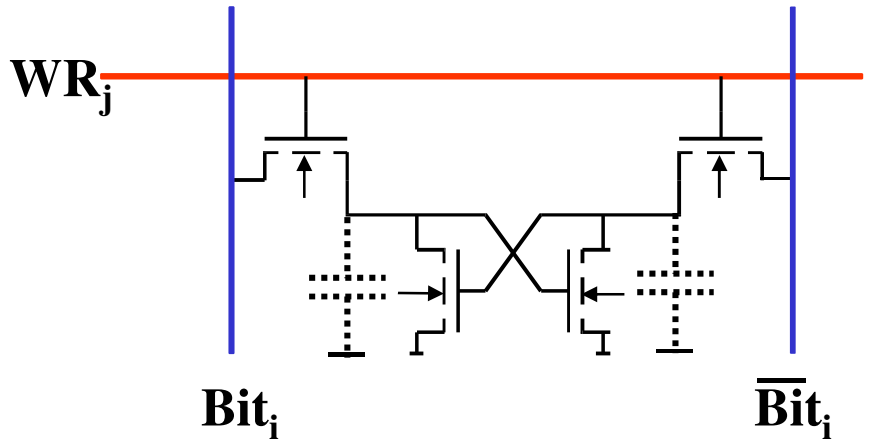
4T- SRAM-Cells



+ smaller area ?
- static current

Static 4-Transistor-RAM-Cell

RAM-Cells - Dynamic

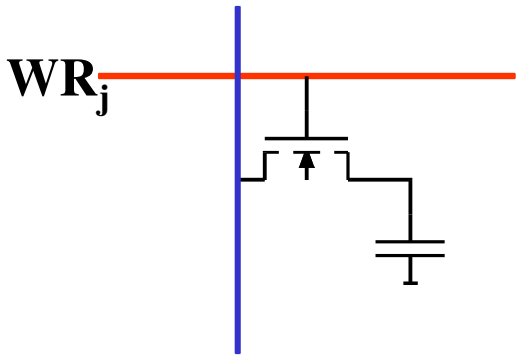


Dynamic 4-Transistor-RAM-Cell

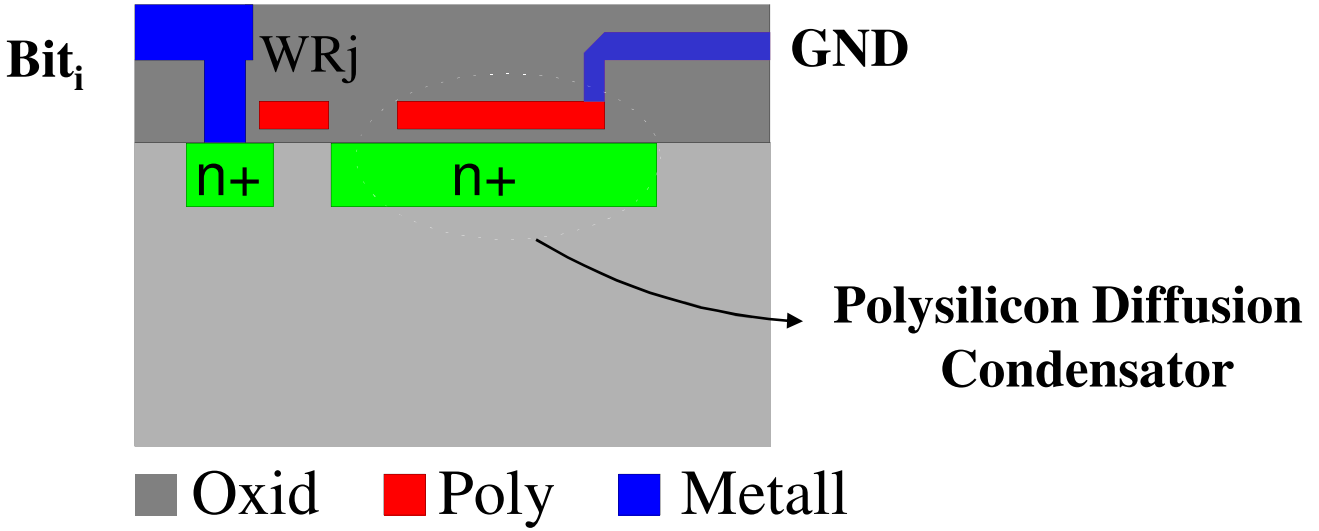
+ smaller area
- „refresh“ necessary

How could the cell be minimized ?

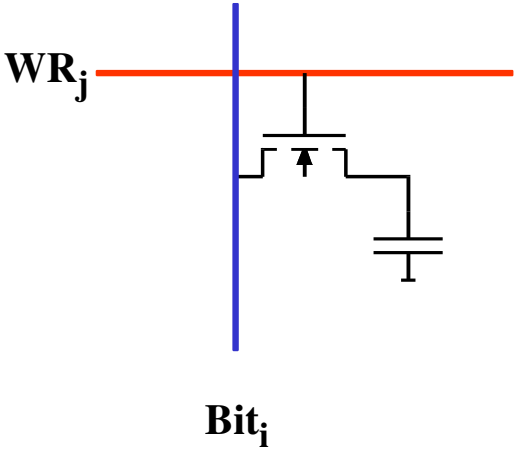
Dynamic 1-Transistor-RAM-Cell

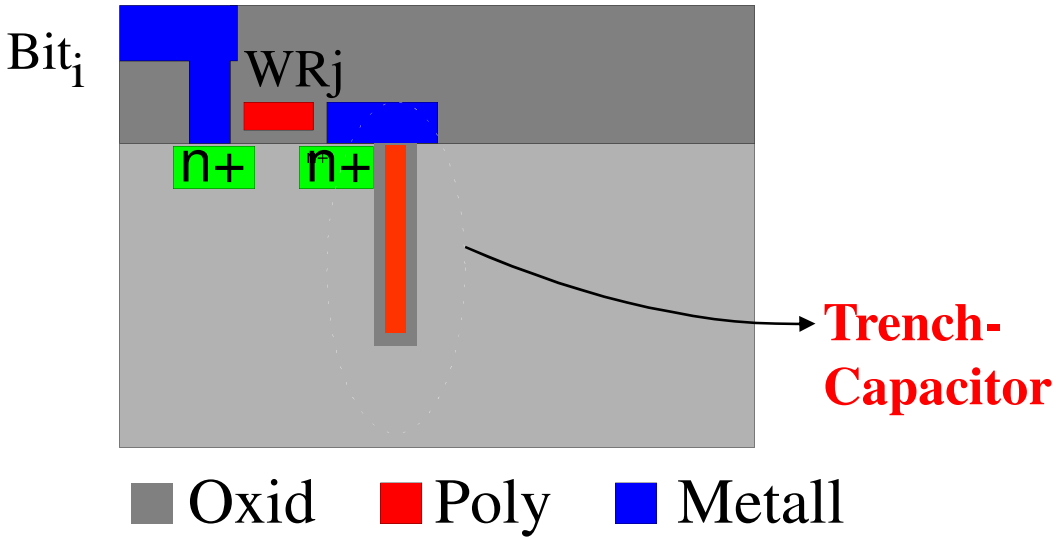


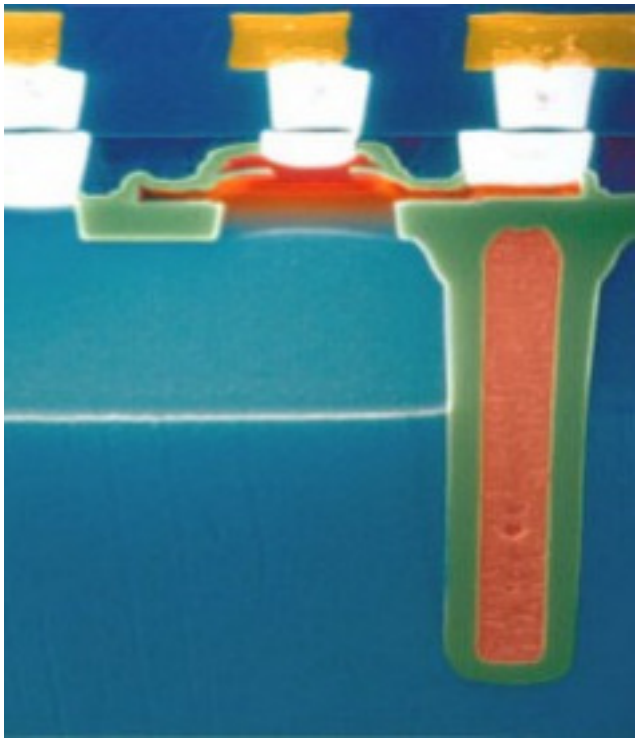
+ smaller area
- susceptible to disburtance
- loss of charge
  while reading



Trench-Condensator Realizations of Dynamic 1-Transistor Cell







A specific (Trench-) Process required.

NVM: Non-Volatile Memory

RAM: no storage, once the supply is interrupted.
ROM: not programmable.

NVM: non-volatile memory

Previous name:	PROM (Programmable ROM) EEPROM (electrically erasable PROM)
Current name:	OTP (one-time programable) MTP (many-time programable)
Special Process:	Flash Memory

Basic principle of NVM

Floating Gate as Memory

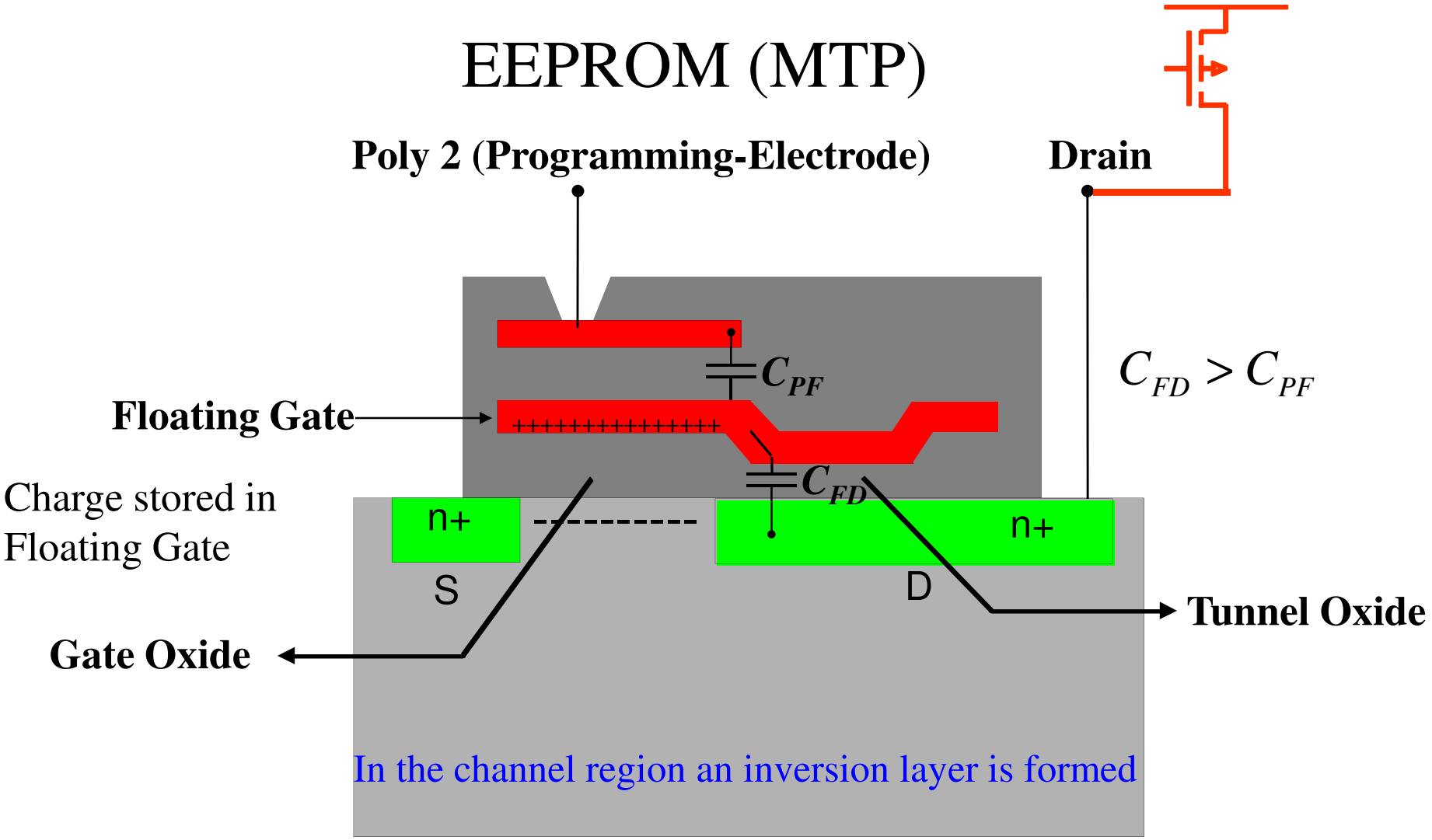
Programming by high electrical field in oxide
(Fowler-Nordheim Tunnel effect, Hot Carrier Injection)

Reading by cell current

Specifics of NVM

Programming / Method:	High voltage necessary (e.g.: 7V for 7 nm gate oxide), Defined (slow) Transient
Quality:	Data Retention (e.g. 10 years) Endurance (e.g.: 10 K programming)
Testing:	Programming -> Baking -> Retest
Redundancy:	install more bits, to detect and correct failures

EEPROM (MTP)

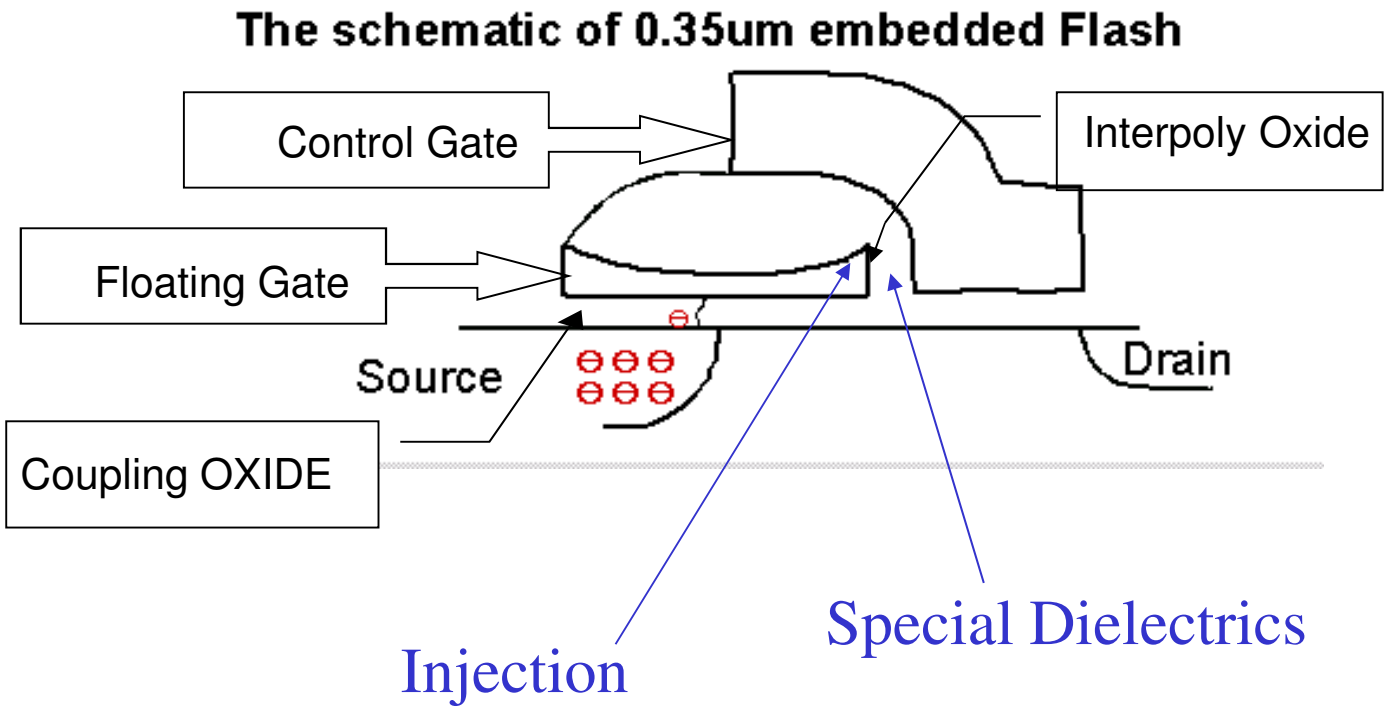


Between Drain- and Programming-Electrode a Programming Voltage Vpp can be applied.

Cell current is read out.

In modern OTP/MTP the cell is realized lateral.

Cross section of a Flash-Storage Cell



Flash needs a special process.

For system on a chip: embedded flash process

(ca. 30 % more expensive than standard CMOS process).

Comparison Memory-Technologies

Type	Density	Access Time	Energy per Bit for writing	Retention	Endurance
SRAM	1	1	1	as long as supply is active	infinite
DRAM	10	20	10	<< 1 second, refresh required	infinite
Flash	30	200000	0.05	10 years	10000

Implementations

- SRAM: Standard CMOS, integrated/embedded
- DRAM: DRAM Process, discrete chip
- Flash: Flash Process, own device

Comparison SRAM – DRAM – NVM

SRAM	+ fast + in standard process always available - large
DRAM	+ high storage density - slow - special process, thus rarely embedded DRAM
OTP / MTP	+ in standard process with medium thick gate oxide (e.g. 7 nm) feasable - very large - extremly slow programming
Flash	+ high storage density - expensive - extremly slow programming