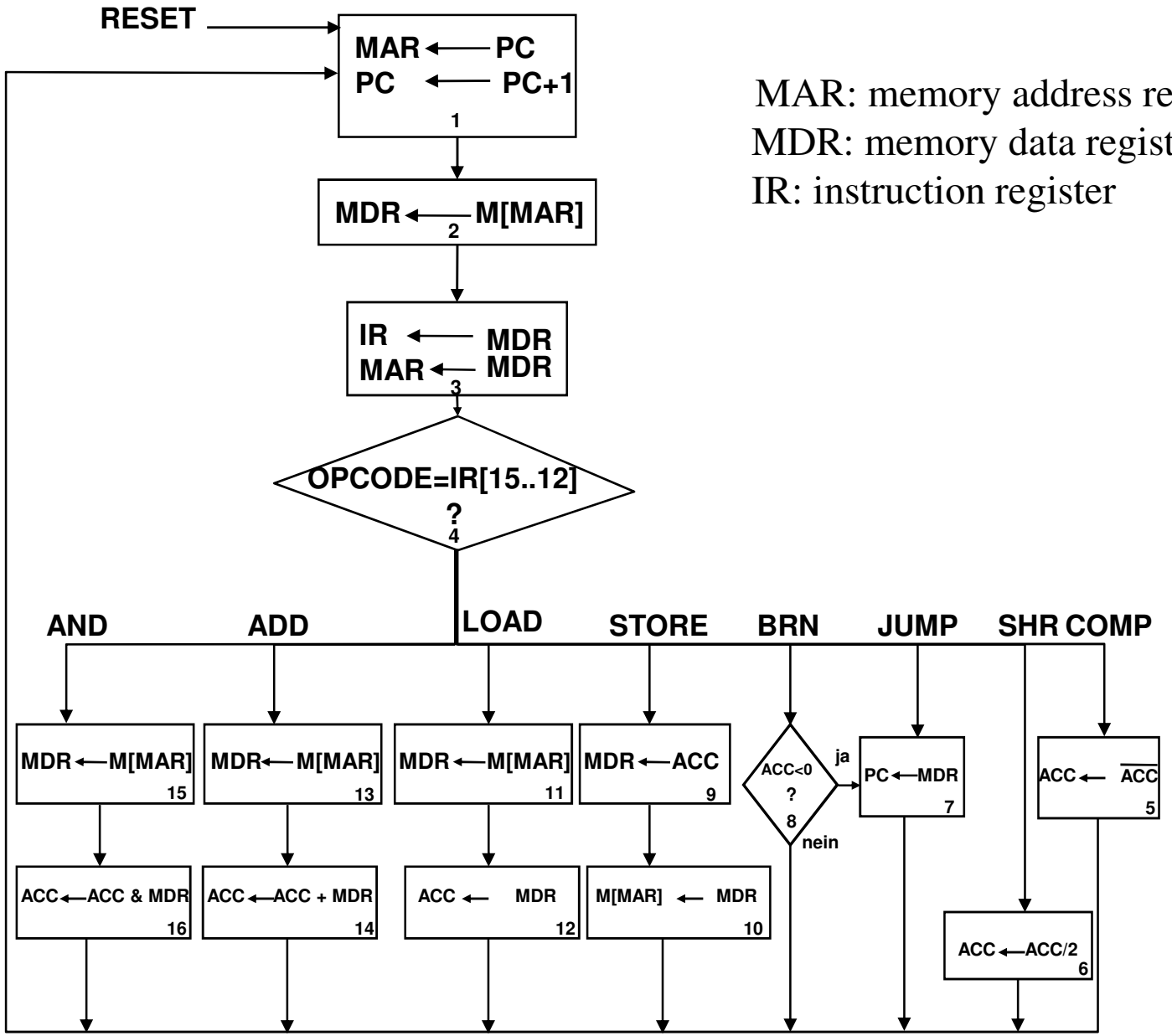
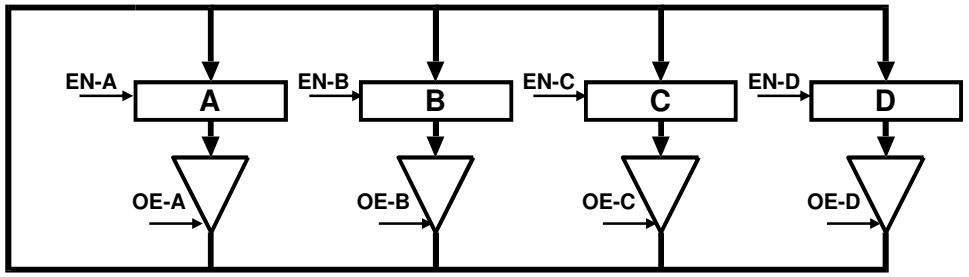
Instruction Flow-Chart



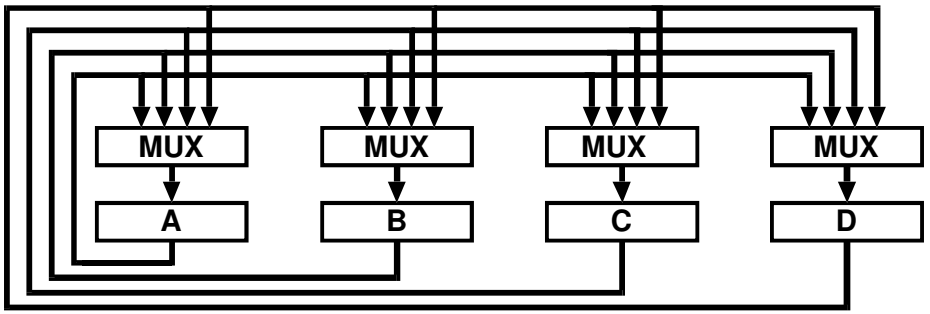
MAR: memory address register
MDR: memory data register
IR: instruction register

Data Path

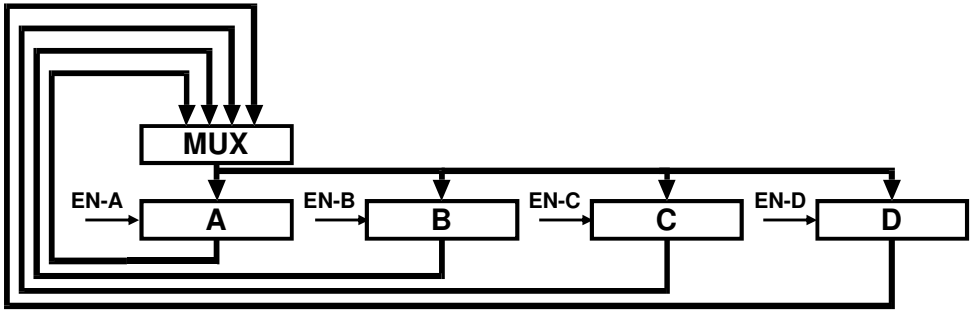
Assumption: 4 Blocks (Register, ALU etc.)



Transfer:
from 1 to 4 $\Rightarrow$ 1 BUS

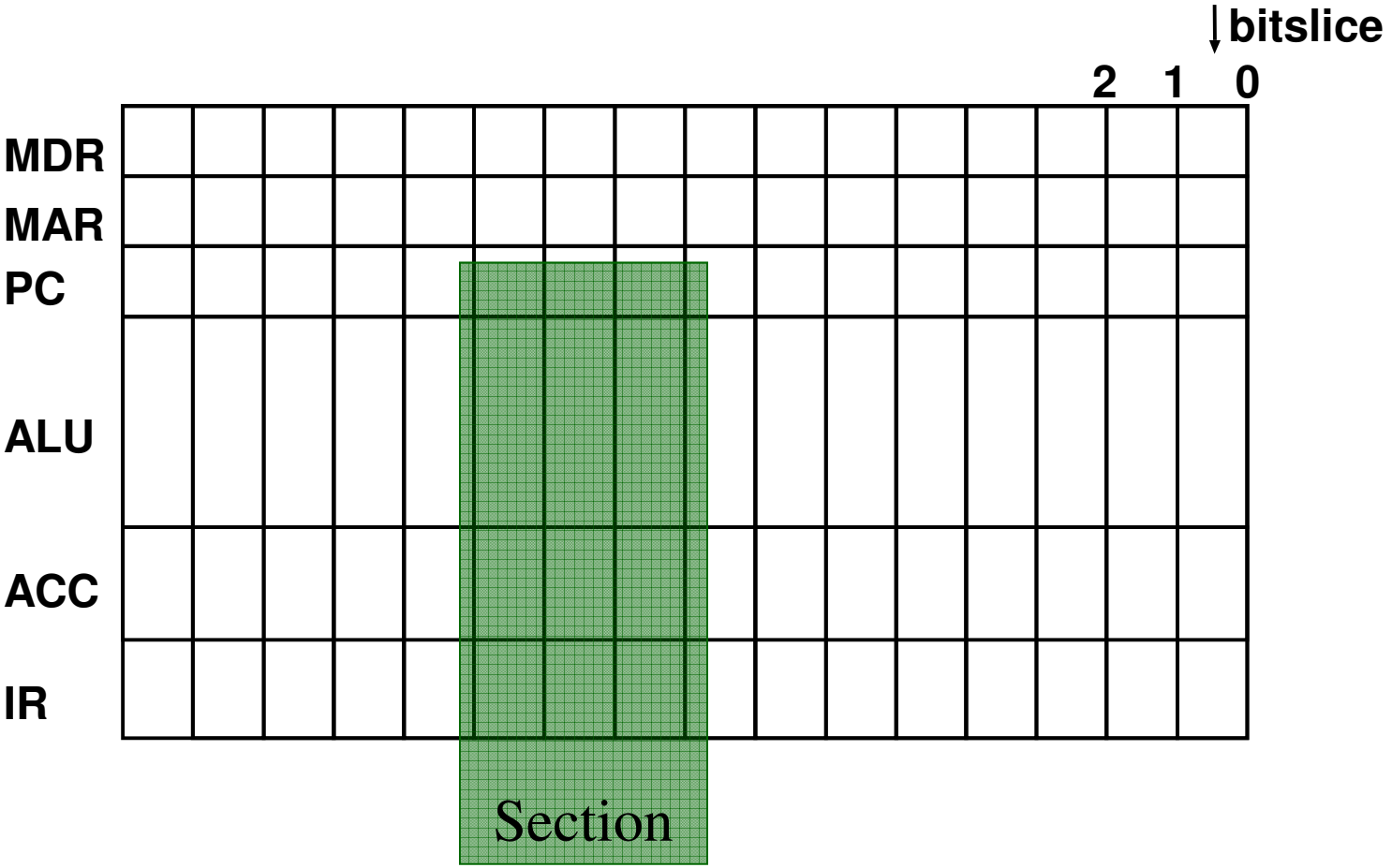


Parallel Transfer possible
(4 x BUS)



1 Transfer / 4 x BUS

Data Path - Floor plan



PC = 12 Bit

MDR = 16 Bit

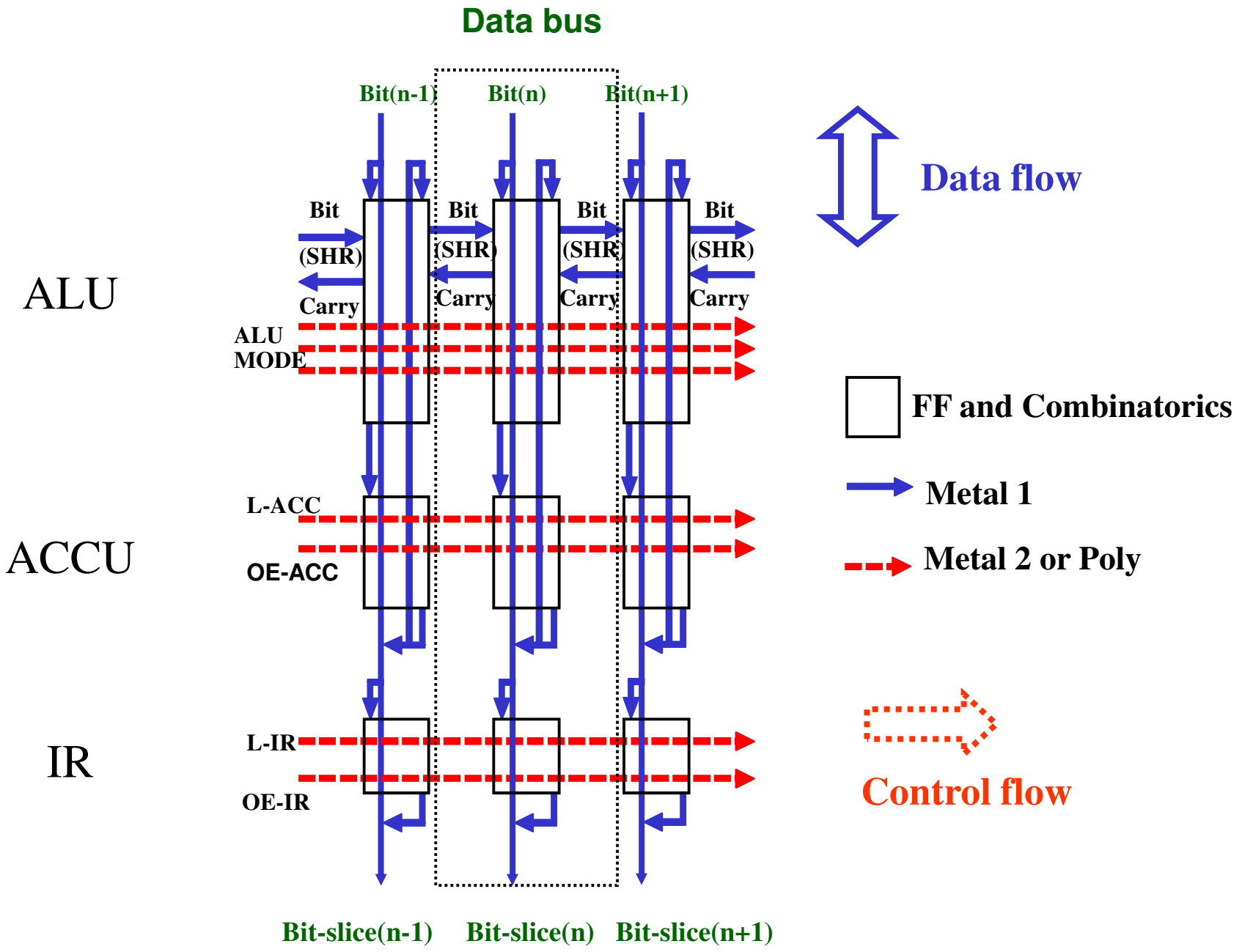
ALU = 16 Bit (Data word width)

ACC = 16 Bit (+Carry)

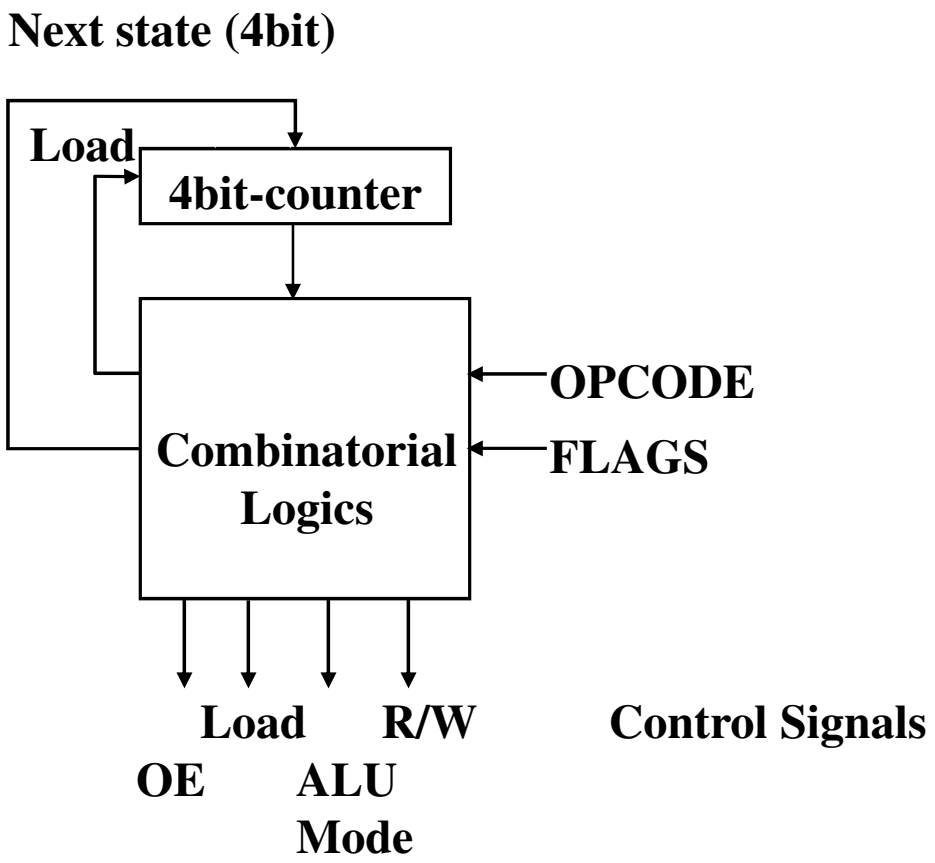
MAR = 12 Bit (16 Bit instruction?)

IR = 16 Bit (4 Bit OpCode)

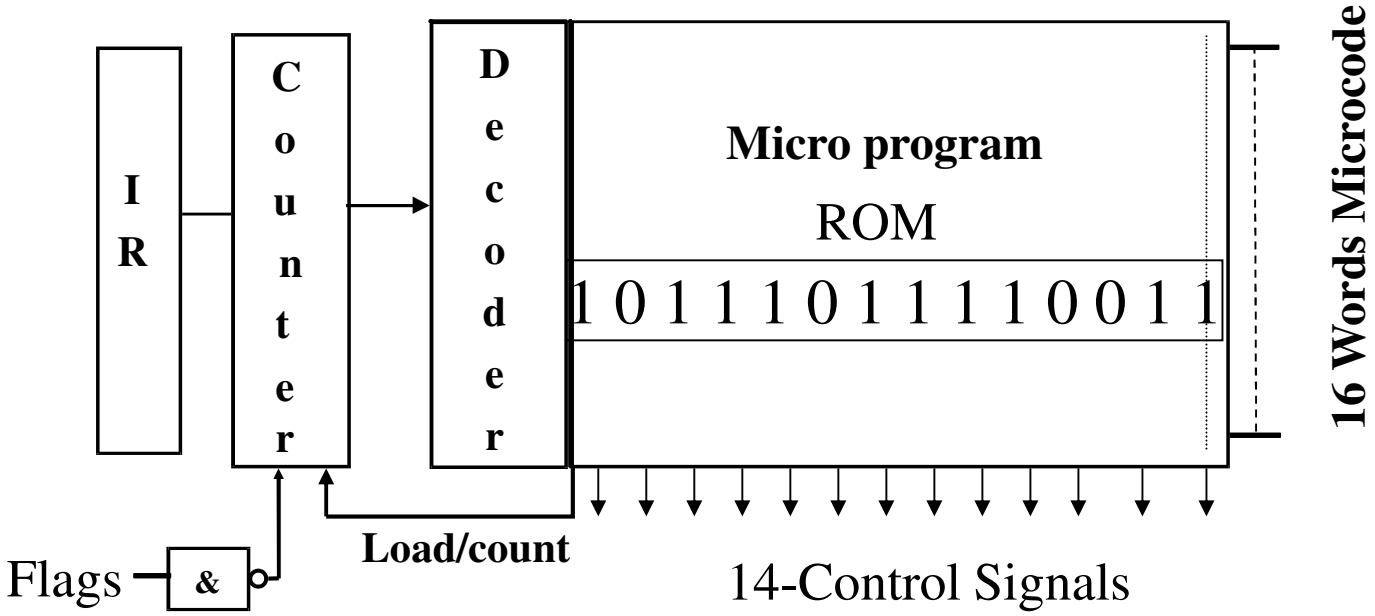
Section of Data Path



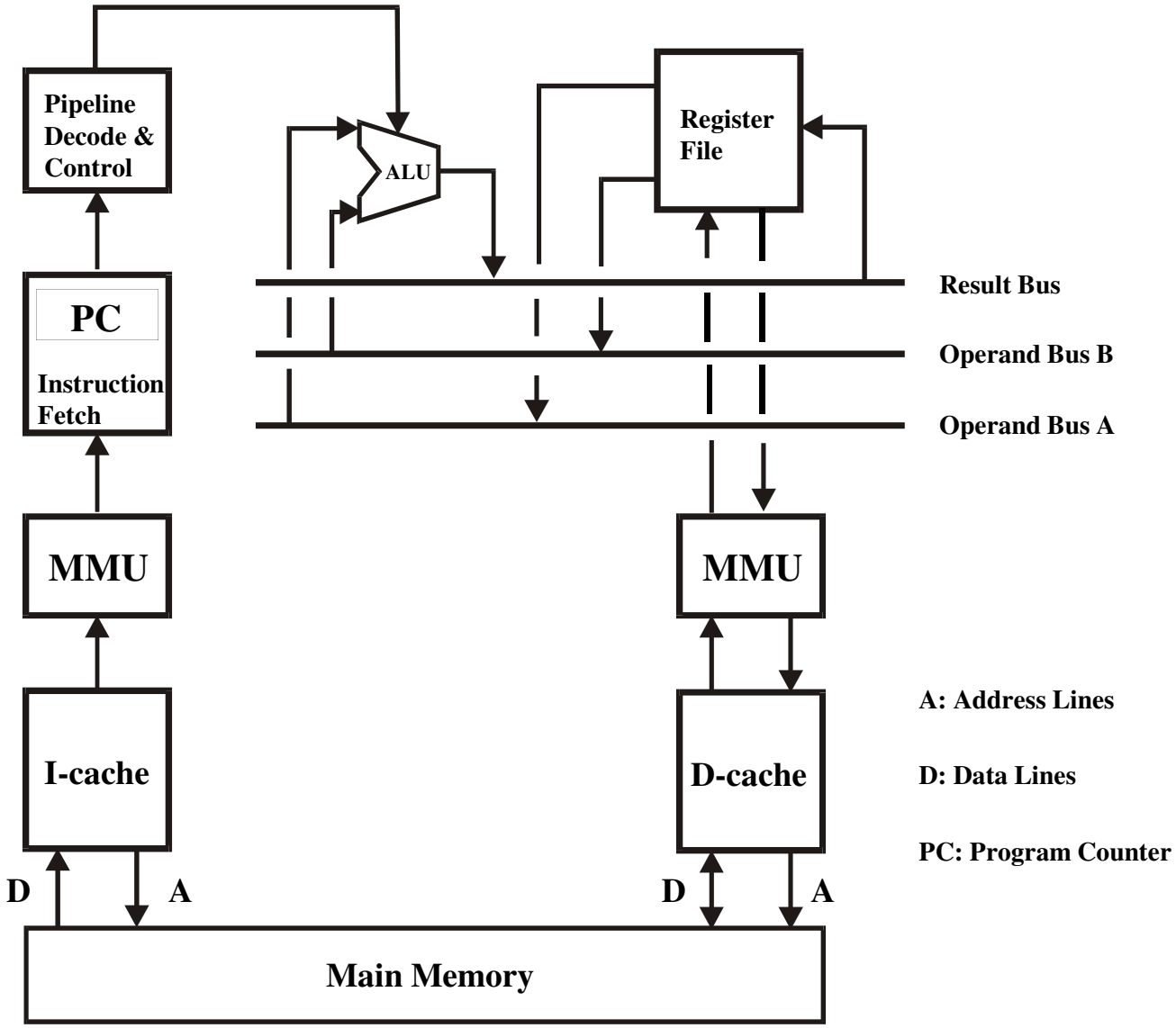
Control Unit for State Machine



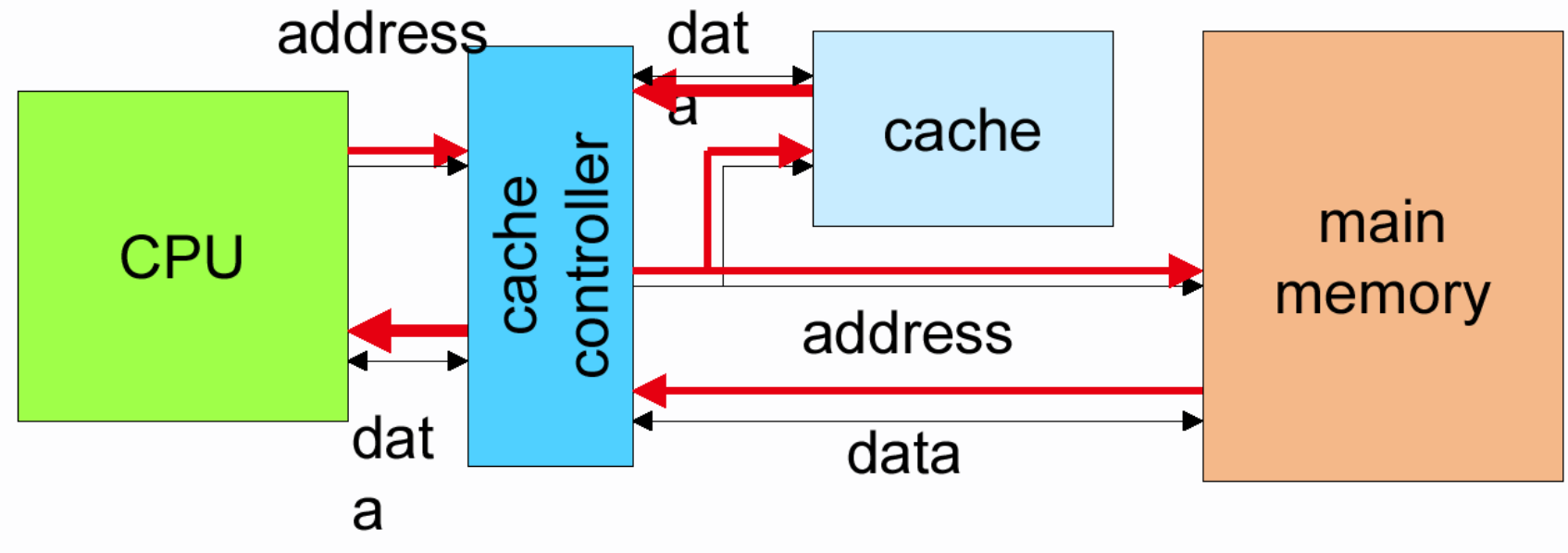
Control Unit with Micro Code-ROM



Data path Organization of a simple Processor



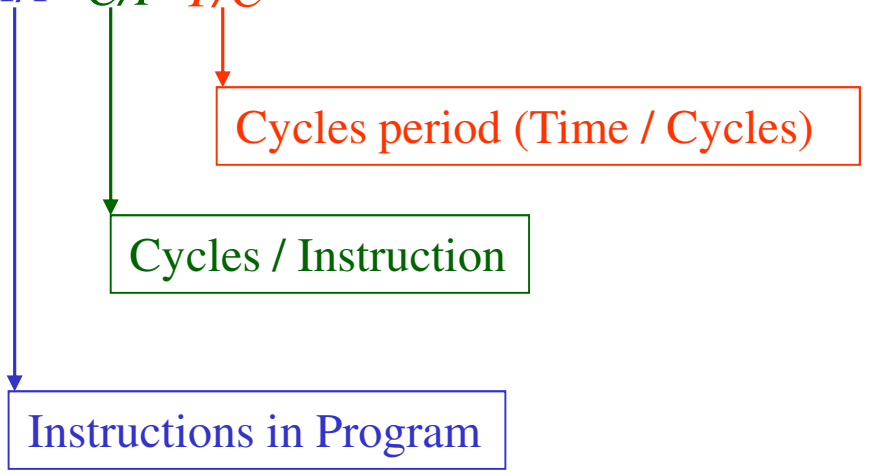
Memory Management Unit (MMU) / Cache Controller



Performance Metrics

Time needed for execution of a program:

Total time= *I/P*•*C/I* •*T/C*



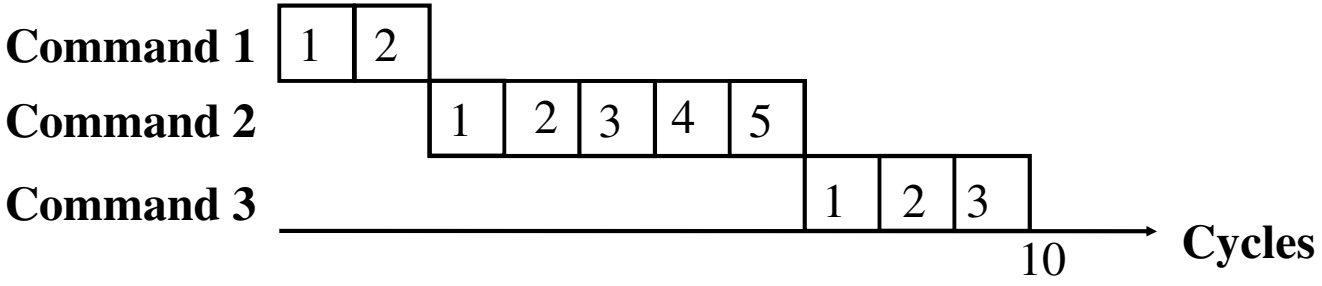
Optimizing Compiler

Pipeline

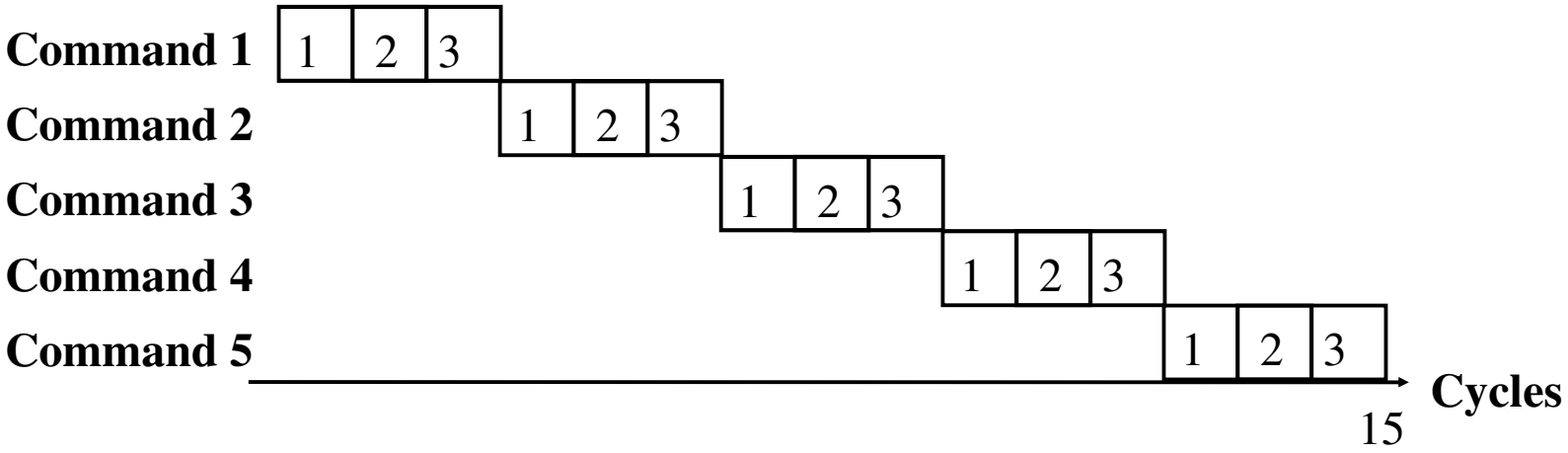
Memory-Hierarchy

Register
Cache
Memory
Disk

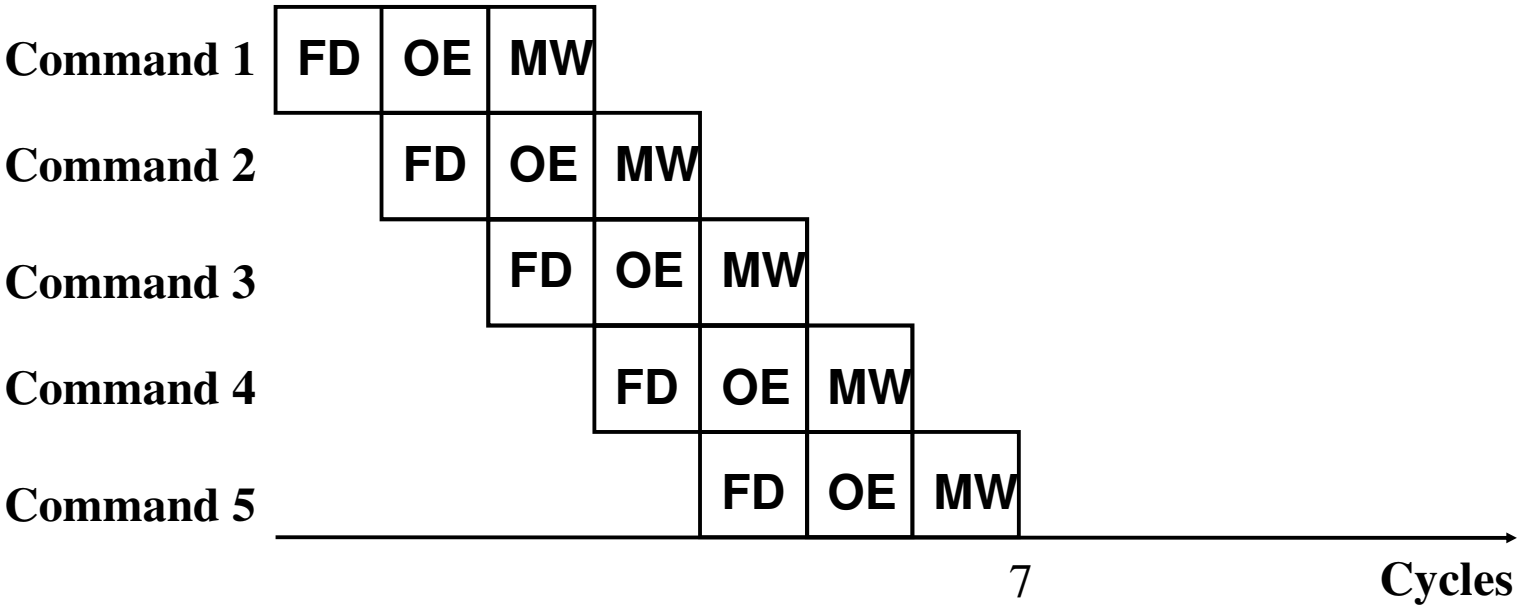
Complex Instruction Set Computer (CISC)

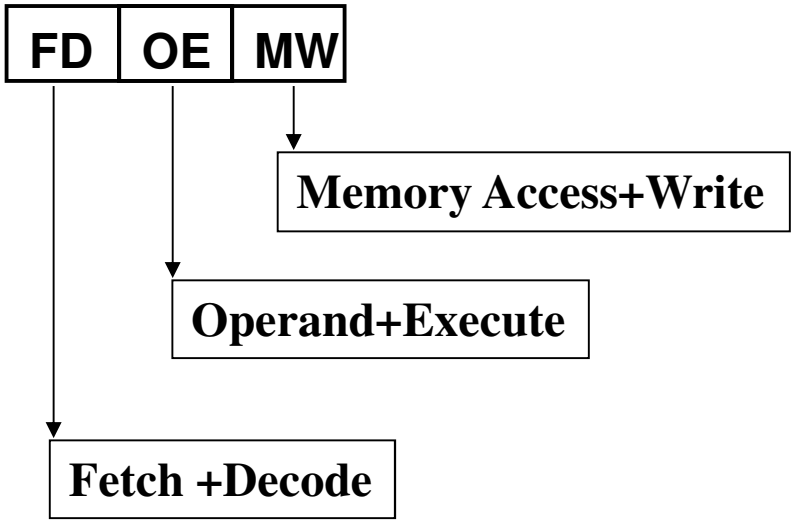


Reduced Instruction Set Computer (RISC)



Pipeline


Command 1
Command 2
Command 3
Command 4
Command 5
FD
OE
MW
7
Cycles


FD
OE
MW
Memory Access+Write
Operand+Execute
Fetch +Decode

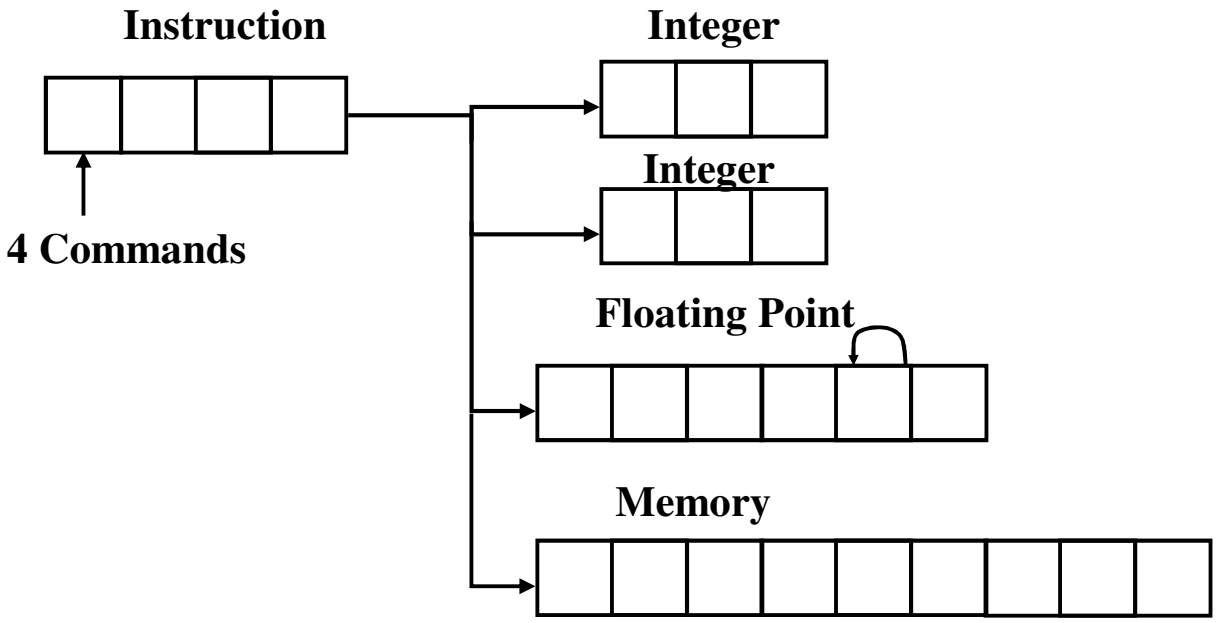
RISC - vs - CISC

	RISC	CISC
Instruction length(Bytes)	Fix	Variable
Instruction cycles	Fix	Variable
Instruction set	Small	Large
Instruction functionality	Simple	Complex
Control	Hardwired (simple)	Microcode (Complex)
Addressing	Register/Register	Complex /Memory
Code-size	Large	Small
Pipeline	Possible	Hardly

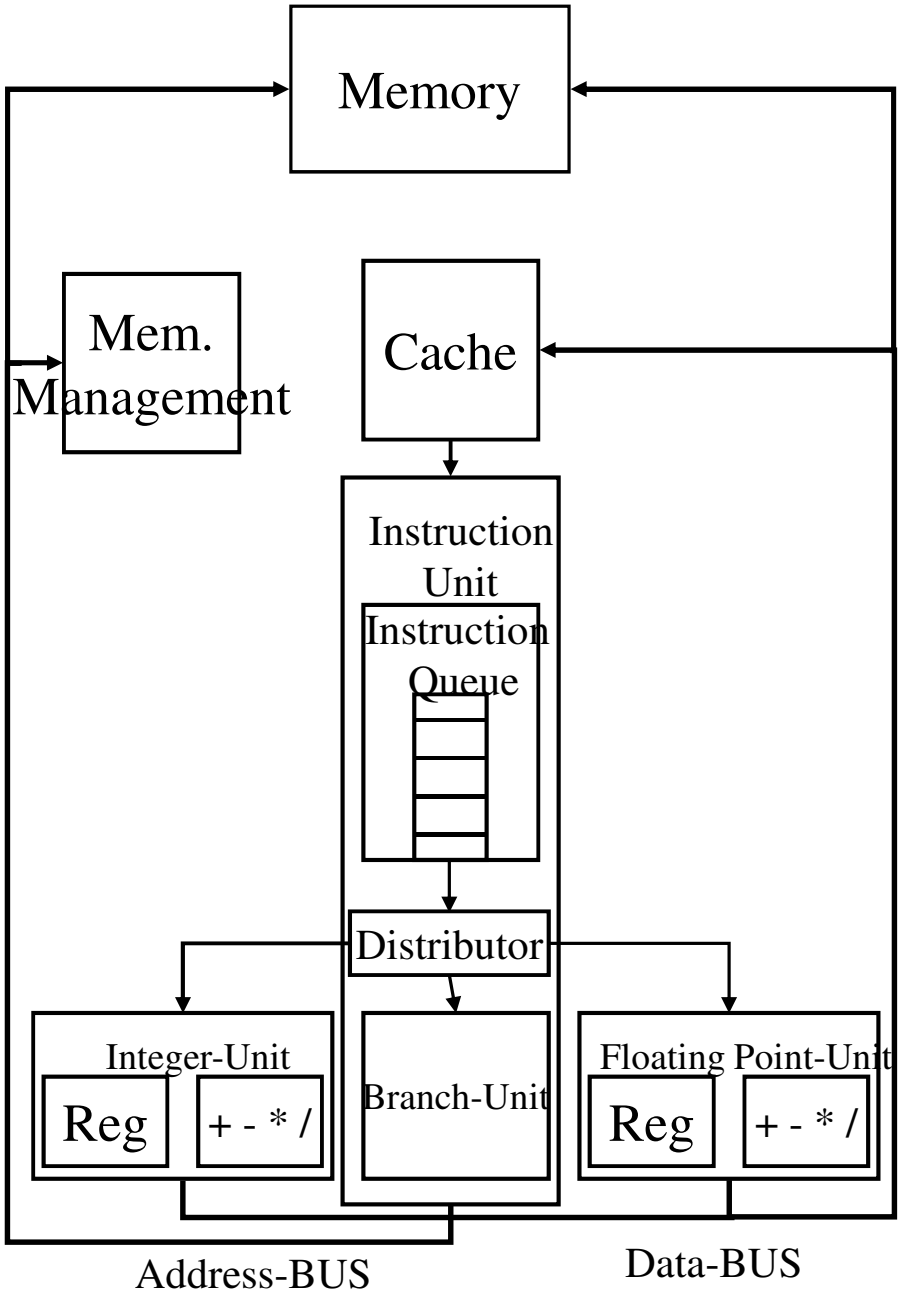
RISC does not really mean „*Reduced Instructions*“

- Complex instructions ➡ Several Cycles
  ➡ Muliplication
  ➡ Floating Point

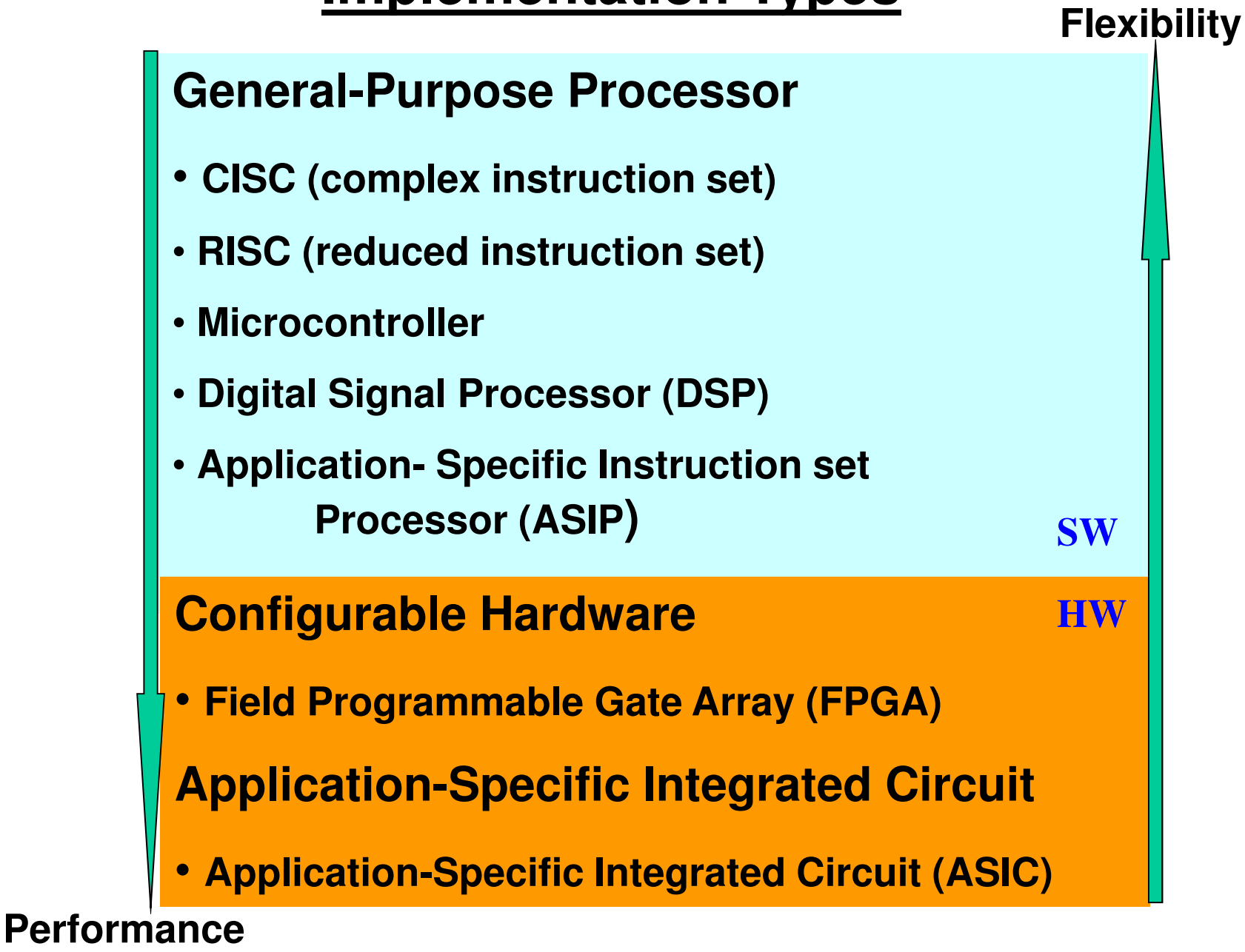
- Parallel processing of several instructions



Modern Processor



Implementation Types



What is System on a Chip?

Complex integrated circuit (IC)

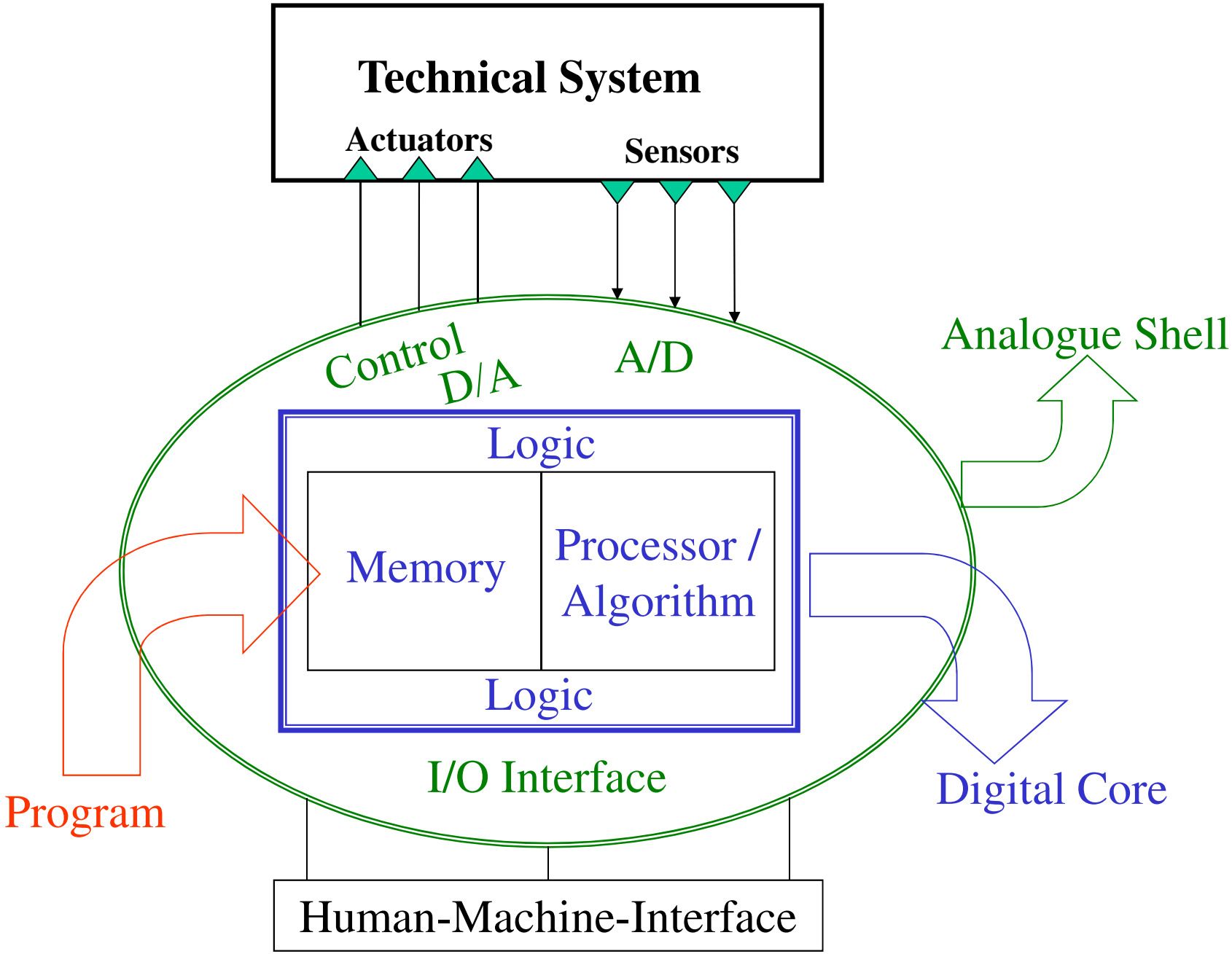
that integrates the major functional elements of a complete end-product into a single chip using intellectual property (IP) blocks:

Programmable processor

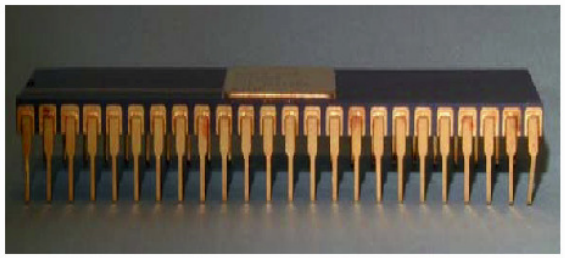
Controllers

Signal processors

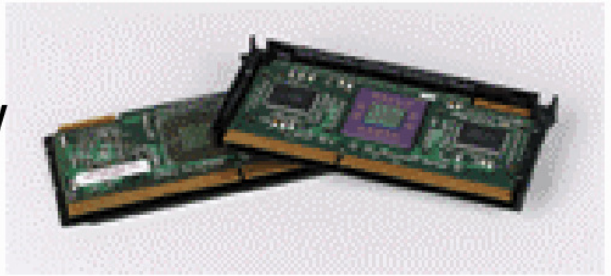
On-chip memory


Technical System
Actuators
Sensors
Control
D/A
A/D
Analogue Shell
Logic
Memory
Processor /
Algorithm
Logic
I/O Interface
Program
Digital Core
Human-Machine-Interface

From Components to IP



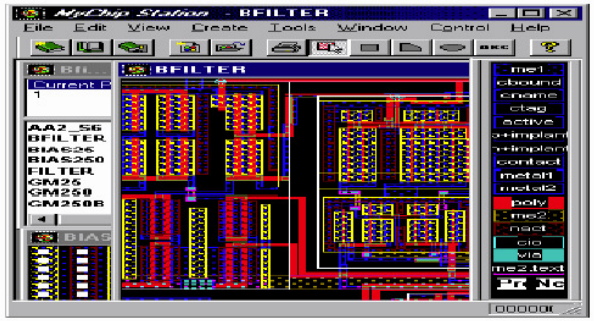
Traditional design flow



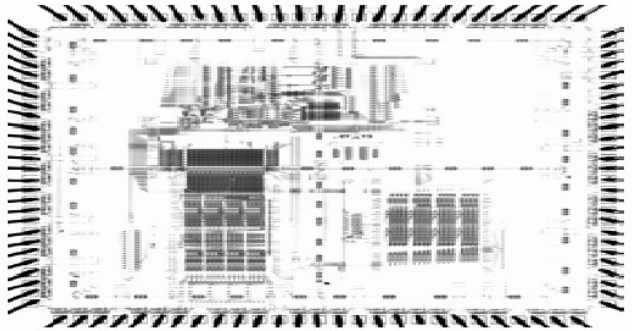
ASIC/CPU Design

Physical components

System-on-a-Board Integration



SOC design flow

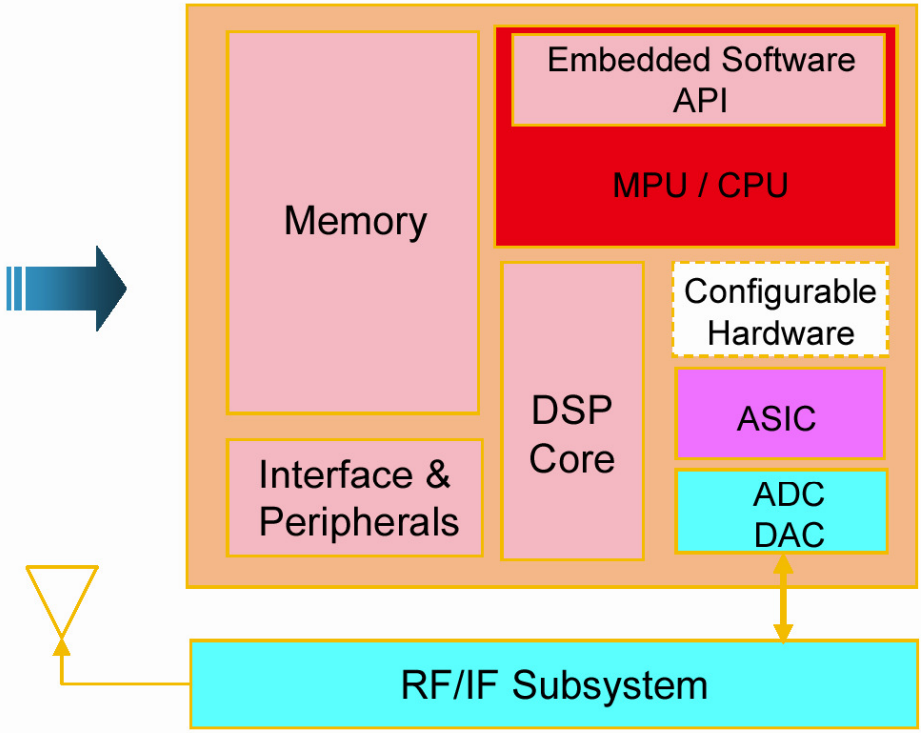


IP Block Authoring

Virtual components

SOC Integration

From Board to Chip



System-on-Board (SoB)

System-on-Chip (SoC)

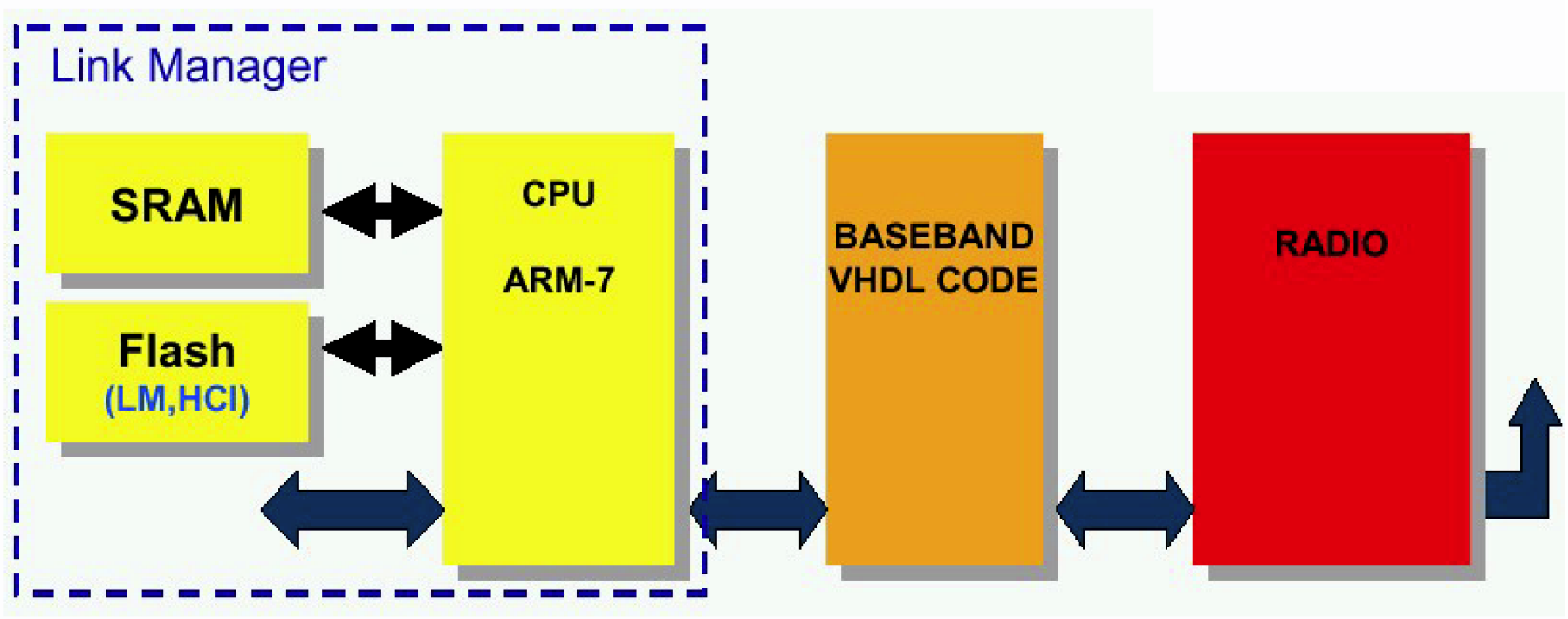
System

A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.

Engineering design perspective for SoC:

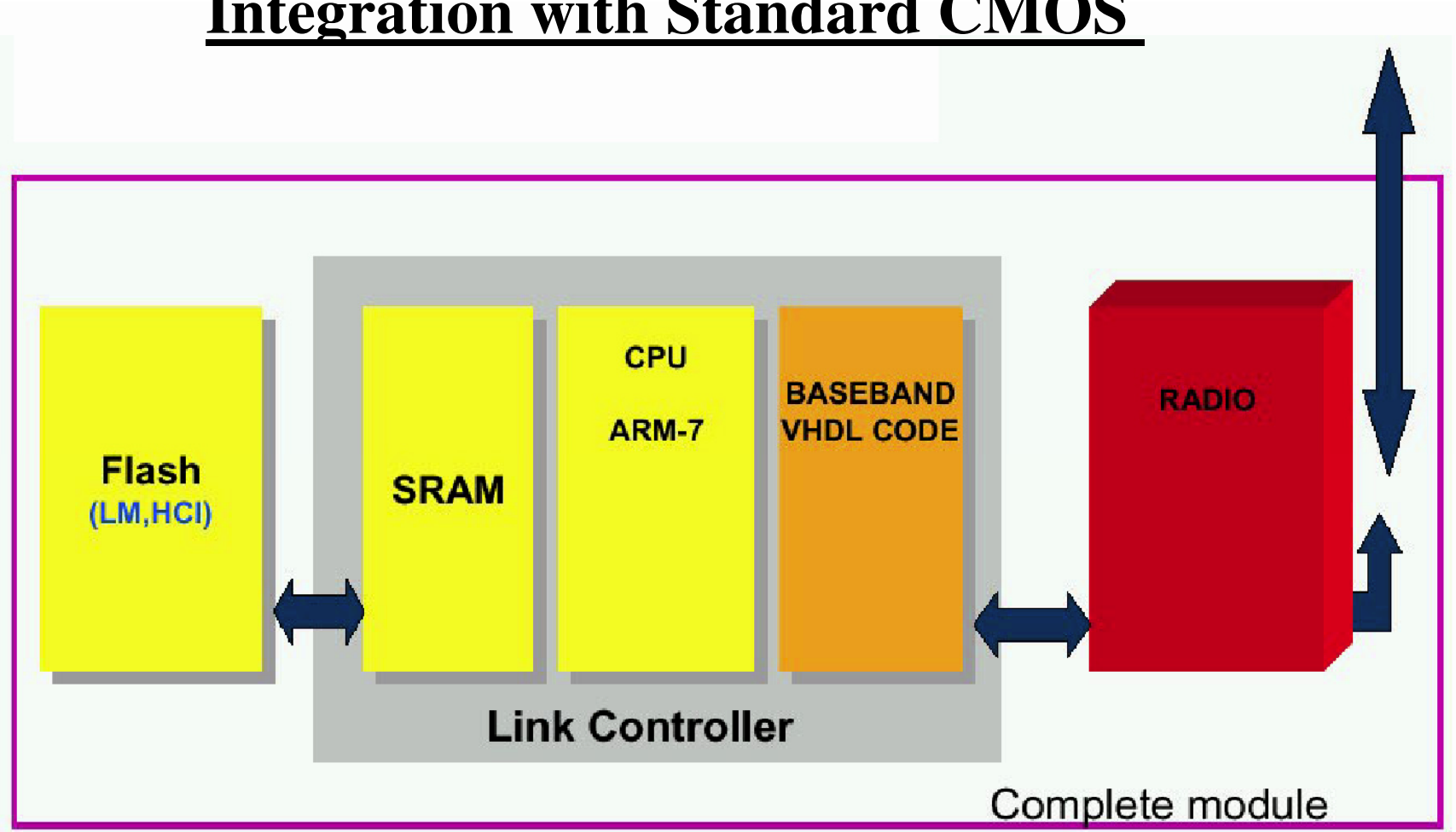
Shrinking product design schedules
Lack of time for product iterations
Complex interoperability standards
Demand for higher performance
Demand for smaller sizes
Demand for lower power

Example Bluetooth Handy



5-chip-solution

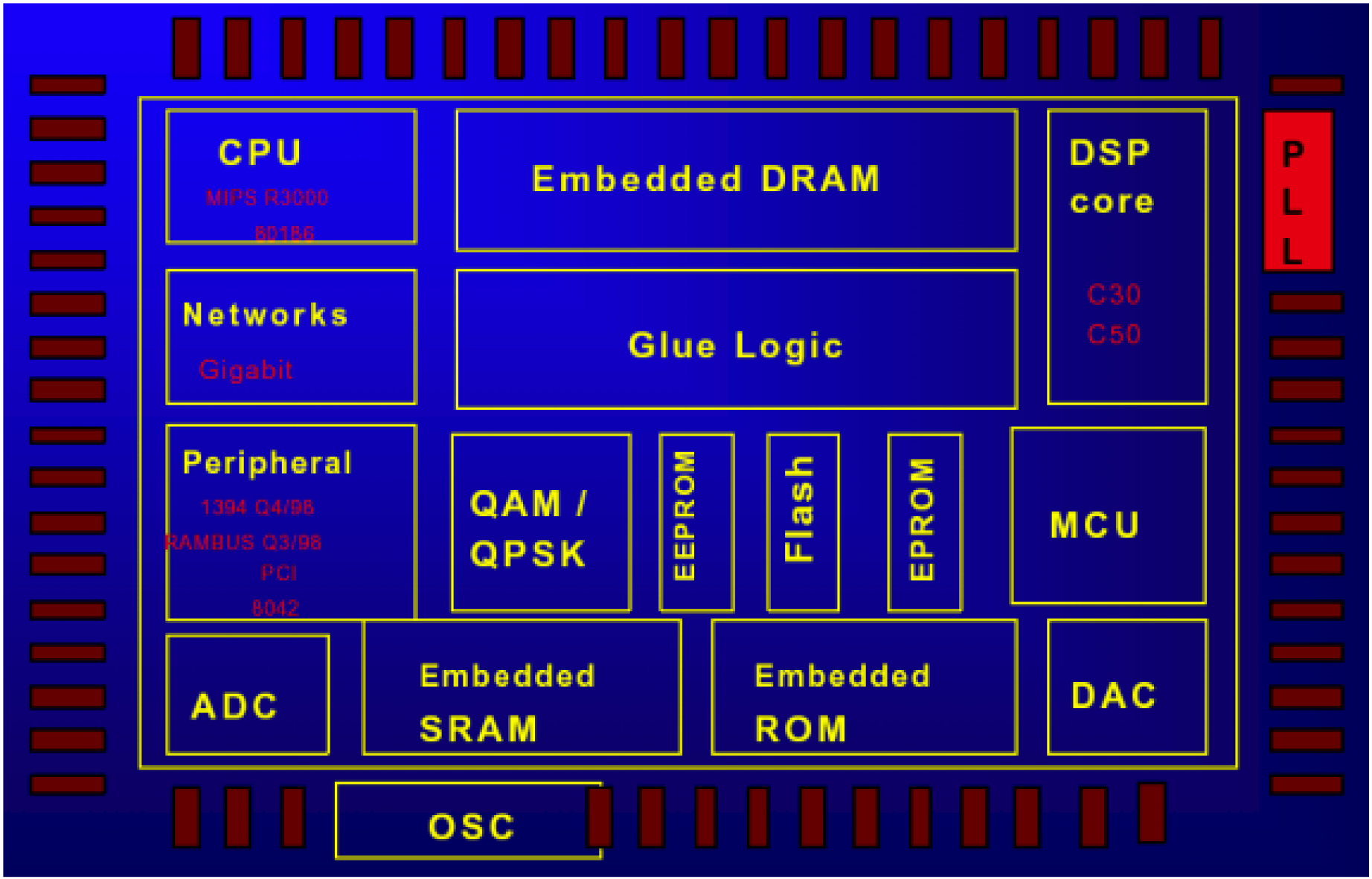
Integration with Standard CMOS



3-chip-solution

One-chip-solution requires a process with Flash and RF

Example for a Network-Processor



Thanks a lot

for your attendance.

See you again in the summer term.