High-Speed Electronic Circuits for 100 Gb/s Transport Networks

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Motivation & Outline

- Develop the “best” high-speed 100G electronics solutions
- Consider SiGe: Inherently fast, high performing, cheap, homogeneous integration (Bi+CMOS), energy efficient
- Outline:
  - State-of-the-art & design considerations
  - Actual SiGe ADC and DAC demonstrators
  - Outlook
Digital (OOK) MUX

- Fastest device on earth
  - InP HBT MUX
    165 Gb/s, 400 mV_{pp}, 1.6 W
  - High speed allows trade-off:
    100 Gb/s, 700 mV_{pp}, 0.8 W
- SiGe speed is sufficient:
  132 Gb/s, 500 mV_{pp}, 1.45 W
- MUX output selector is inherently fast (est circuit)
- Speed supported by $g_m \uparrow$
  $\sim$ gain & output conductance
- CMOS ($g_m \downarrow$) < 50 Gb/s

$$\text{HBT } g_m(I_0) \approx 10 \quad \text{MOS } g_m(\sqrt{I_0})$$
Digital Modulator Driver

- Aim: power + cost saving
- Consider: MZI, $V_{\pi} = 2 \, \text{V}$, push-pull config.
- Direct drive by Power-MUX:
  - ✔ 50 Gb/s, 2 $V_{pp}$ (1998)
    - (Si-bipolar $f_t/f_{\text{max}} = 72/75$ GHz)
- Standard MUX
  - 0.7 $V_{pp}$ @ 100 Gb/s (InP)
  - 0.5 $V_{pp}$ @ 132 Gb/s (SiGe)
  - to be optimized for voltage swing ↑
  - support by next gen. HBT technol.
- Expect > 1 $V_{pp}$ @ 112 Gb/s in SiGe
Analog MUX: DAC

- MUX concept enables very fast SiGe DACs
- Direct push-pull modulator drive with 2 $V_{pp} @ 30$ GHz possible
Linear Modulator Driver

- Higher speed: parasit. C ↓
- Distributed amp. concept
  - L compensates for C
  - but HBTs input impedance is not pure C
- Emitter degeneration
  - input impedance → C
  - linearizes
  - gain ↓ but x 2 is suffic.
- Next. gen. SiGe HBTs:
  - BVCEO → 1 V, but ...
  - push-pull > 2V_{pp} @ 40GHz
(Transimpedance) Amplifier

- Parallel feedback ($R_F$):
  - low ohmic $Z_{in}$
  - linearization
- Volt. amp. must have
  $\text{mag}(G_V) \uparrow + \text{phase}(G_V) \downarrow$
  $\rightarrow$ HBTs ($g_m \uparrow$)
- Parasitics for $f \uparrow$:
  $Z_{in} \rightarrow 50 \, \Omega$ (34 dBΩ)
- Use 50-Ω pre-amp. w/o feedback $\leftrightarrow$ noise
Autom. Gain Control (AGC) Amp

- How to get P↓?
  - next SiGe tech. is 3x faster
  - integrate with ADC
    - saves 50-Ω I/O
    - digital peak detect.
- $f_{\text{intens}} < f_{\text{AGC}} < \min(f_{\text{sig}})$?
- DSP task: gain dependency?

source: Sewiolo et al. [45]
OOK: CDR & DeMUX

- Marginal 112 Gb/s performance → High power consumption (2..5 W)
- Improvements by
  - next gen. HBT technol. \((f_t/f_{\text{max}} \approx 300 / 500 \text{ GHz})\)
  - “novel” circuit concepts
- “Novel”:
  - don't squeeze out bipolar transistor performance \((g_m \uparrow \rightarrow \text{operating currents } \uparrow)\)
  - Look how CMOS copes with it's inherent worse \(g_m\)!
Analog RX: ADC

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>SiGe</th>
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<tbody>
<tr>
<td>sampl. rate</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>ENOB</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>power diss.</td>
<td>++</td>
<td>----</td>
</tr>
<tr>
<td>bandwidth</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>DSP noise</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>tech. outlook</td>
<td>-/O</td>
<td>+</td>
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</table>

- Next generation
  - 60/120 GS/s,
  - ENOB > 5/4
  - BW > 25/50 GHz
  - P = 2 W ?
- DSP < 45 nm

next gen. targets?

448 Gb/s!!!

InP HBT
SiGe HBT
CMOS

DSP noise

60/120 GS/s
5 bit
4 bit
3 bit
210/285
150/240
120/250
65nm
65nm
65nm
65nm
65nm
65nm
65nm
SiGe HBT DAC / ADC demonstrators

- Part of European 100GET R&D program to
  - evaluate pros, cons and future potential of SiGe converters
    - main target: **maximum bandwidth**
    - enable system design and transmission experiments
      - main target: **real time operation**
  - Real time interface to commercially available FPGAs
    - Xilinx Virtex 4/5: 24 Transceivers up to 6.5 Gb/s
    - Altera Stratix 4: 24 ... 48 Transceivers up to 8.5 Gb/s
  - 6 bit resolution; 4 times multiplexed interface = 24 lanes
    - Virtex4/5: 26 GS/s (+ overclocking)
    - Stratix 4: 34 GS/s
30 GS/s 6 bit ADC demonstrator

- Transparent sampling 0-30 GS/s → scalable: trade speed against power
- Differential or single-ended operation and ac-coupling possible
- 282 mV_p-p full-scale input
- Input bandwidth ≈ 22 GHz
- On-chip 100 ps clock phase shifter
  - Sampling point adjustment
  - Interleaving of 4x 30GS/s ADCs
- Pure SiGe HBT cell based design $f_T/f_{max}$, 200/250 GHz.
ADC static performance

- Optimization of automatic calibration currently in progress:
  - to adjust threshold, offset, and gain of converter stages
ADC dynamic performance

- Measurement: SR=30 GS/s
- ENOB estimate based on only 16 samples
- Measurement with internal RC-Oscillator (noise)

- Design issue: ringing of ADC output drivers to FPGA
- Max. interface rate limits sampling rate to 18 GS/s
- Workaround: store 16 samples to internal memory → transfer data via serial low speed register interface to PC → calculate sine-fit (IEEE-STD-1241)
ADC power dissipation map

- 10.0 W total power diss.
- ADC core power:
  - 0.65 W input amp
  - 1.96 W T&H
  - 0.43 W Clock
  - 1.80 W ADC
  - 4.84 W
- Logistics + auxiliary:
  - 4.16 W FPGA I/O
  - 1.16 W Aux.
- Savings:
  - safety margins
  - circuit concepts
  - next Bi+CMOS gener.
- Target: 4 W (65 GS/s, 25 GHz BW, 5 ENOB)
30 (38) GS/s 6 bit DAC demonstrator

- CML output, on-chip 50-Ω term.
- Full-scale output programmable: 0.25 ... 0.9 mV_{pp} (single ended)
  0.50 ... 1.8 V_{pp} (differential).
- Bandwidth: > 25 GHz.
- Speed limit at 28 GS/s
  (7 Gb/s overclocked Virtex 4 I/Os)
- 38 GS/s core speed
  (but timing issue to be solved)
- Pure SiGe HBT cell based design
  f_T/f_{max}, 200/250 GHz.
DAC power dissipation map

If all blocks powered on:

- 8.4 W FPGA I/O+Sync.
- 1.3 W Regs., cal, ...
- **3.3 W High speed circ.**
- 13.0 W Total

High speed consumes „only“ ¼ of total power

¾ of total power due to „logistics“ at 7.5...15 Gb/s.
DAC performance

• INL measurement
• DC Ramp
• DAC running at 30 GS/s
• Code applied via internal register
• 50-Ω DC termination

![Integral Nonlinearity vs. code (test mode)](image)

- Dynamic FOMs @ 28GS/s measured up to
  - Nyquist freq. (14 GHz)
  - full meas. BW (26.5 GHz)

<table>
<thead>
<tr>
<th>DAC @ 28 GS/s</th>
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<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>875 MHz</td>
</tr>
<tr>
<td>0-26 GHz</td>
</tr>
<tr>
<td>SINAD [dB]</td>
</tr>
<tr>
<td>ENOB [bit]</td>
</tr>
<tr>
<td>SFDR [dB]</td>
</tr>
<tr>
<td>SNR [dB]</td>
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<tr>
<td>THD [dB]</td>
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Module #2

INL ( LSB )

1250mVpp
1600mVpp
1900mVpp

• INL measurement
• DC Ramp
• DAC running at 30 GS/s
• Code applied via internal register
• 50-Ω DC termination

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DAC transient performance

- **FOM 1: glitches**
  - MSB-1 ↔ MSB
  - all along a ramp
  - step response (over/undershoot)
  - shall be $< \pm \frac{1}{2}$ LSB

- **FOM 2: rise/fall time**
  - full scale step
  - shall reach $\pm \frac{1}{2}$ LSB of start and end values

- Is this really required?
ADC/DAC boards for real time experiments

Xilinx ML424 Board with Virtex4-FX140

48 RF-cables for 24 differential SerDes links

15 GHz Clock → input

Reference clock (:40) for FPGA is generated by the DAC

DAC module

\[30 \text{ GS/s output}\]
Outlook on high-speed electronics

• **Rethink transceiver partitioning**: combine, relax and release functions/tasks and performance
  – direct MZM drive, integrate AGC, adaptive DAC step size ...
  – DSP algorithm. to consider electronics as a part of the channel

• **Next generation BiCMOS technology**: speed x2
  – trade speed against power efficiency
  – novel concepts to replace $g_m$-driven performance

• **SiP**: no need for low-ohmic 50-Ω TML interfaces
  – Use simple + high ohmic, high-speed interfaces

• **3-D TSV interconnects** becomes cheap Si standard assembly (DRAM, MEMS). Tend: 2000 I/Os, $\varnothing=2\mu m$, $l=20\mu m$
  – combine best CMOS and SiGe technologies → Bi+CMOS